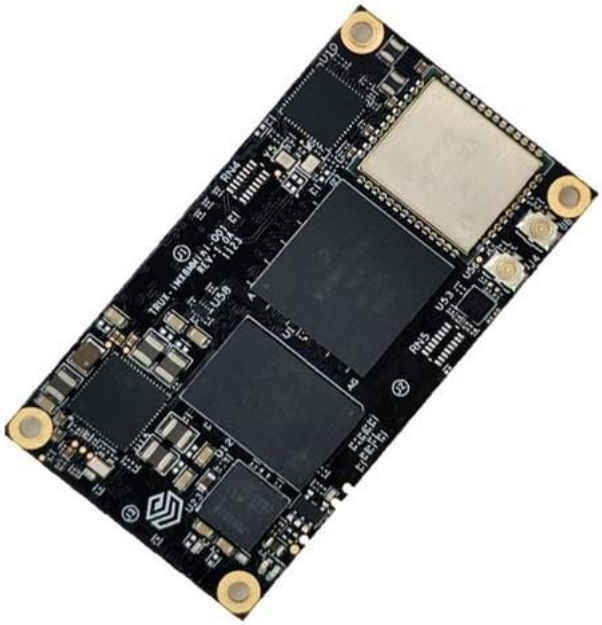
Hardware Development User Guide

For TRUX SOM

TRUX-iMX8MMini-Q01



Rev 1-1

Status: Released

Contents

Revision History

Revision	Date	Notes
1.0	November 30th 2022	Draft Release
1.1	July 27th 2023	Released

Acronyms and Abbreviations

Term	Meaning
I2S	Inter IC Sound
GPIO	General Purpose Input Output
B2B	Board to Board
LPDDR	Low Power Double Data Rate
eMMC	Embedded Multimedia Card
SD	Secure Digital
HDMI	High-Definition Multimedia Interface
USB	Universal Serial Bus
PCI	Peripheral Component Interconnect
MIPI	Mobile Industry Processor Interface
DSI	Display Serial Interface
CSI	Camera Serial Interface
I2C	Inter Integrated Circuit
ECSPI	Enhanced Configurable Serial Peripheral Interface
JTAG	Joint Test Action Group
UART	Universal Asynchronous Receiver Transmitter
CAN	Controller Area Network
PMIC	Power Management Integrated Circuit
SNR	Signal to Noise Ratio
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
SPDIF	Sony / Philips Digital Interface
SAI	Switch Abstraction Interface
CRC	Cyclic Redundancy Check
RGMII	Reduced Gigabit Media Independent Interface
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
ICMP	Internet Control Message Protocol
COL	Computer Oriented Language
PWM	Pulse Width Modulation
FIFO	First In First Out
OTG	On The Go
RDC	Resource Domain Controller
TZ	Trust Zone
OCRAM	On-chip RAM
HAB	High Assurance Boot
CAAM	Cryptographic acceleration and assurance
SNVS	Secure non-volatile storage
RTC	Real-time clock
SJC	Secure JTAG controller
ENET	Ethernet

1. Introduction

1.1 Purpose

This document is the hardware user manual for TRUX-iMX8MMini-Q01 System on Module. The SOM is designed using NXP's i.MX 8M Mini application processor. The user manual describes detailed information about SOM & its usage.

1.2 Overview

The TRUX-iMX8MMini-Q01 CPU module is an NXP i.MX 8M Mini Quad processor implementing quad Arm Cortex–A53 core-based system on module operating up to 1.8GHz speed and Cortex-M4 core processor for low power processing with Linux OS. It is cost effective and power efficient. It offers a wide range of interfaces such as GPIOs, SAI, SPI, I2C, UART buses, high speed USB 3.0 interfaces, SD-card, camera & display interface with industry standard.

The SOM is compact in size and integrated with on-board PMIC, 16GB eMMC Flash, 4GB LPDDR4, Audio codec and WIFI / BT well suited for general embedded, Industrial control, consumer and IoT applications. TRUX-iMX8MMini-Q01 is an extreme performance, low-power SoM that provides 4K industry-leading video, voice, audio processing capabilities.

1.3 Specifications

Features:

- CPU: i.MX 8M Mini: Cortex-A53 upto 1.8GHz and Cortex-M4 upto 400MHz
- PMIC: ROHM BD71847AMWV-E2

Memory:

- LPDDR4 (1 - 4GB)
- eMMC (8 – 32 GB)
- EEPROM (2K)

External Memory:

- SD Card (up to 32GB)

Audio Codec, Stereo:

- Resolution: 24 bits
- Conversion Rate: 96KHz
- SNR: 90dB ADC / 100dB DAC

Power Supply:

- 3.5V to 5V

OS support:

- Yocto Dunfell (Kernel v5.4.142)
- Android - Android 11.0.0_1.0.0 (kernel 5.4.47)

Security:

- Secure OS with Hardware Crypto Authentication chip

Form factor:

- 55.1 mm x 30.2 mm

Supported temperature:

- 0°C to +70°C Commercial
- -40°C to +85°C Industrial

Peripherals:

- LPDDR4 x1 (32bit LPDDR4-3200)
- eMMC x1 (8 bit)
- SD x1 (4bit)
- Ethernet x1 (RGMII with IEEE 1588 STD)
- USB 2.0 (OTG) x2
- PCI Express x1 (Gen 2.0)
- MIPI DSI x1 (lane4)
- MIPI CSI x1 (lane4)
- I2C x4
- SPI x3
- SAI x6
- JTAG x1
- UART x4
- GPIOs x65
- Boot Mode Signals
- Digital Audio serial interface: I2S (SAI) x4, S/PDIF x1

2. Block Diagram

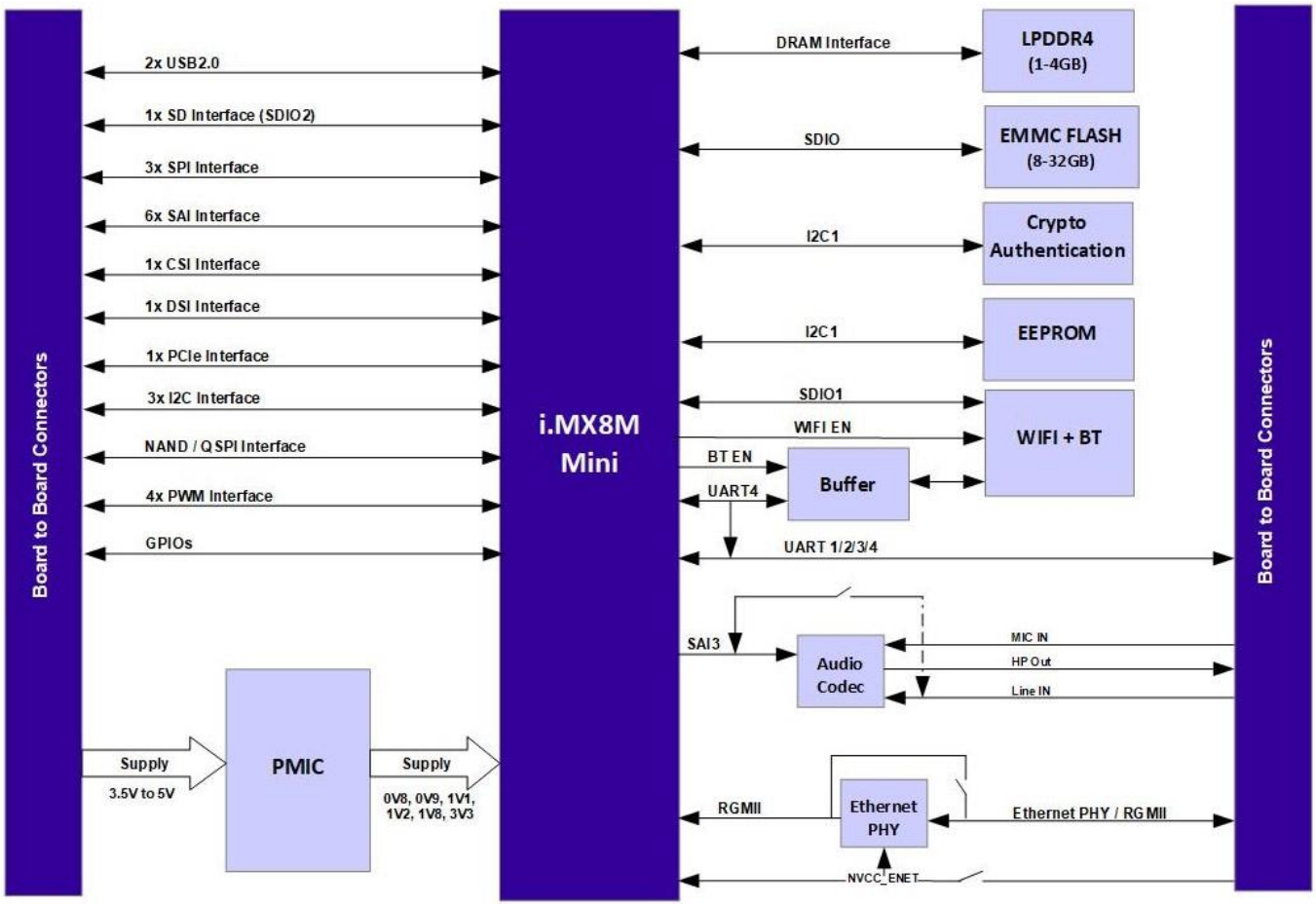
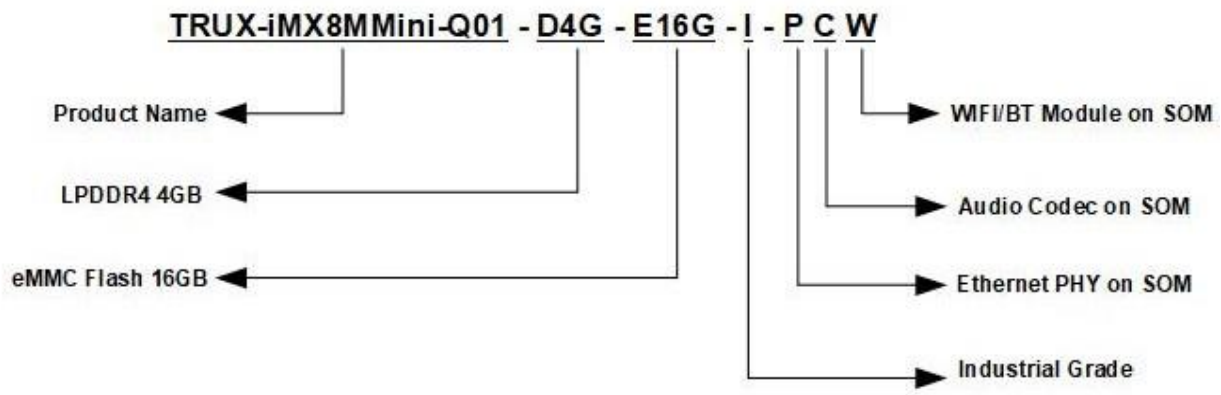


Figure1: Block Diagram of TRUX-iMX8MMini-Q01 SOM

3. TRUX-iMX8MMini-Q01 SoM Configuration

Below figure gives Part number description of TRUX-iMX8MMini-Q01-D4G-E16G-I-PCW



4. Processor Overview

4.1 Architecture of i.MX 8M Mini Processor

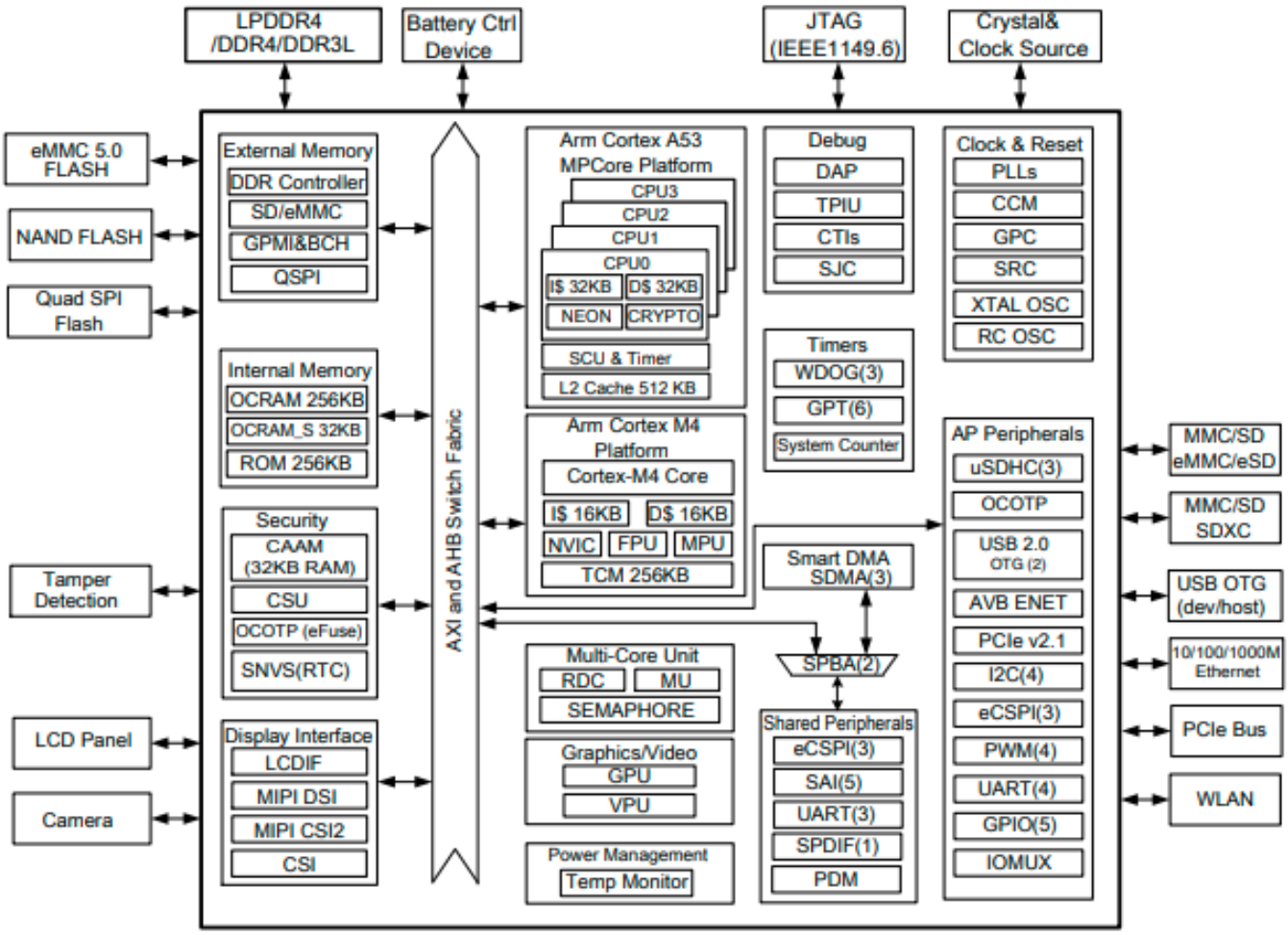


Figure2: Block diagram of i.MX 8M Mini Processor

4.2 Part Number Nomenclature

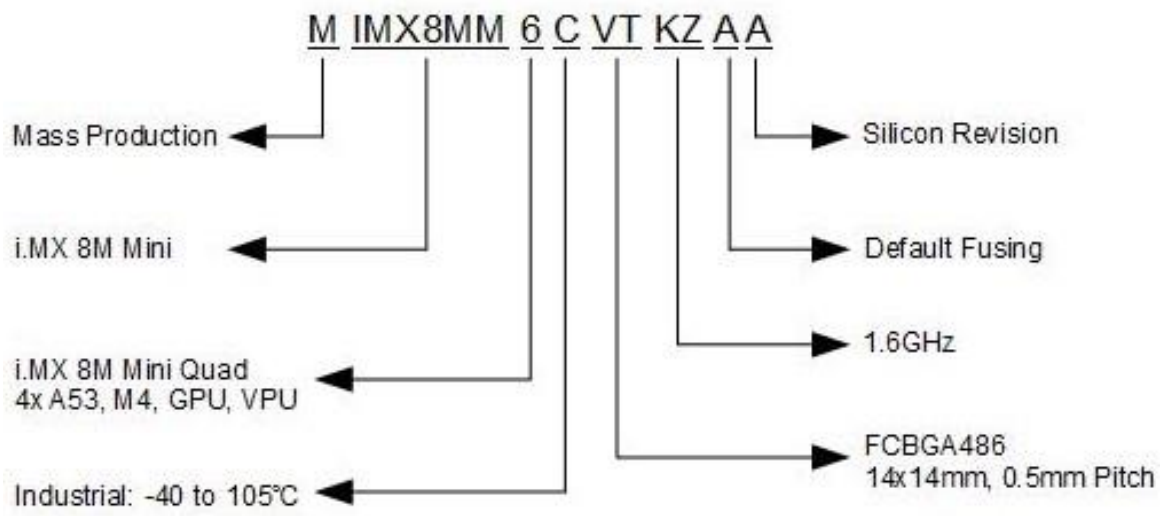


Figure3: Part number description of i.MX 8M Mini Processor

4.3 Specifications of i.MX 8M Mini Quad processor

The i.MX 8M Mini Media Applications Processor is built to achieve both high performance and low power consumption and relies on a powerful fully coherent core complex based on a quad Cortex-A53 cluster with video and graphics accelerators.

The i.MX 8M Mini Family provides additional computing resources and peripherals:

• Advanced security modules for secure boot, cipher acceleration and DRM support

• General purpose Cortex-M4 processor for low power processing

• A wide range of audio interfaces including I2S, AC97, TDM and S/PDIF

• Large set of peripherals that are commonly used in consumer/industrial markets including USB 2.0, PCIe and Ethernet

- **Application Processor**: 4x Cortex - A53 core platforms up to 1.6 GHz per core, 1x Cortex – M4 core up to 400MHz.
- **Graphic Processor**: 3D GPU (1x shader, OpenGL ES 2.0), 2D GPU
- **Video Playback**:
  - 1080p60 VP9 Profile 0, 2 (10-bit) decoder, HEVC/H.265 decoder, AVC/H.264 Baseline, Main, High decoder, VP8 decoder
  - 1080p60 AVC/H.264 encoder, VP8 encoder
- Display: 1x MIPI DSI (4-lane) with PHY

- Audio: 5x SAI (12Tx + 16Rx external I2S lanes), 8ch PDM input
- Dual Camera Interfaces: 1x MIPI-CSI (4-lanes each)
- USB: 2x USB 2.0 OTG controllers with integrated PHY
- PCIe: 1x PCIe 2.0 (1-lane) with L1 low power substates
- Ethernet: 1x Gigabit Ethernet (MAC) with AVB and IEEE 1588, Energy Efficient Ethernet (EEE) for low power
- OS: Linux®, Android™
- **Security**
  - RDC – Resource Domain Controller: Supports 4 domains and up to 8 regions
  - Arm TrustZone including the TZ architecture: ARM Cortex-A53 MPCore TrustZone support
  - On-chip RAM (OCRAM) secure region protection using OCRAM controller
  - High Assurance Boot (HAB)
  - Cryptographic Acceleration and Assurance Module (CAAM) o Support Widevine and PlayReady content protection
- **Power Management**
  - Temperature sensor with programmable trip points
  - Flexible power domain partitioning with internal power switches to support efficient power management

5. SoM Components

5.1 LPDDR4

TRUX-iMX8MMini-Q01 SOM supports 1GB - 4GB LPDDR4 RAM (32bit LPDDR4-3200) memory. To support this, it uses a single LPDDR4 IC. This chip operates at 1.1V voltage level.

5.2 eMMC Flash

The TRUX-iMX8MMini-Q01 SOM supports 8GB- 32 GB eMMC Flash as boot device. This is connected to i.MX 8M Mini CPU and operates at 1.8 Voltage level.

5.3 PMIC

TRUX-iMX8MMini-Q01 SOM supports BD71847AMWV-E2 PMIC for on-SOM power management. The BD71847AMWV-E2 is a Power Management Integrated Circuit (PMIC) designed specifically for i.MX 8M Mini application processors.

The BD71847AMWV-E2 PMIC provides all required power to i.MX 8M Mini CPU and all on SOM peripherals. 3.5 -5V power input from B2B connector comes to PMIC as an input & PMIC generates all other required powers internally on SOM itself.

5.4 Audio Codec

TRUX-iMX8MMini-Q01 SOM provides high performance audio as it contains ultra –low power stereo CODEC (WM8904), optimized for portable audio applications.

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Integrated FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 3 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel
- Ground-referenced headphone driver
- Ground-referenced line outputs

5.5 Crypto Authentication

TRUX-iMX8MMini-Q01 SOM has facility to integrate Secure OS with Hardware Crypto Chip. The ATECC608B (default not populated on SOM) is a member of the Microchip CryptoAuthentication™ family of high-security cryptographic devices, which combine world-class, hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols. The ATECC608B provides security enhancements.

6. Board to Board Connector

The TRUX-iMX8MMini-Q01 exposes three 90-pin board-to-board connectors. The recommended mating connector is Hirose P/N: **DF40C-90DS-0.4V (51)**.
Below is a list of all i.MX 8M Mini pins, ALT0 to ALT6 and alternate ICs which are available on B2B connectors.

6.1 B2B J1 Pin Function List

B2B Connector Pin Number	B2B Connector Pin Name	Pull up /Pull down on SOM	i.MX 8M Mini Alternate Signals	i.MX 8M Mini Alternates	i.MX 8M Mini Ball Number	Alternate ICs Signals Name	Alternate ICs Pin Number
J1.1	GPIO1_IO00		REF_CLK_32K	ALT5	SOC.AG14	GPIO1_IO00	AP6275S.31
J1.2	ETH_TRX1_P		ENET_TD1	ALT0	SOC.AF26	ETH_TRX1_P	RTL8211FS.5
J1.3	NC						
J1.4	ETH_TRX1_N		ENET_TD0	ALT0	SOC.AG26	ETH_TRX1_N	RTL8211FS.6
J1.5	LED_LINK10_100		ENET_TXC	ALT0	SOC.AG24	LED_LINK10_100	RTL8211FS.35
J1.6	ETH_TRX0_N		ENET_TD2	ALT0	SOC.AG25	ETH_TRX0_N	RTL8211FS.3
J1.7	LED_LINK1000		ENET_RXC	ALT0	SOC.AE26	LED_LINK1000	RTL8211FS.36
J1.8	ETH_TRX0_P		ENET_TD3	ALT0	SOC.AF25	ETH_TRX0_P	RTL8211FS.2
J1.9	LED_ACT		ENET_RX_CTL	ALT0	SOC.AF27	LED_ACT	RTL8211FS.37
J1.10	ETH_TRX2_P		ENET_RD0	ALT0	SOC.AE27	ETH_TRX2_P	RTL8211FS.7
J1.11	NC	PU 1.5K					
J1.12	ETH_TRX2_N	PD10K	ENET_RD1	ALT0	SOC.AD27	ETH_TRX2_N	RTL8211FS.8
J1.13	NC						
J1.14	ETH_TRX3_P	PD 10K	ENET_RD2	ALT0	SOC.AD26	ETH_TRX3_P	RTL8211FS.10
J1.15**	NVCC_SNVS_1V8				POWER IN		Run at 1.8V level!
J1.16	ETH_TRX3_N	PD 10K	ENET_RD3	ALT0	SOC.AC26	ETH_TRX3_N	RTL8211FS.11
J1.17	I2C4_SCL		GPIO5_IO20	ALT5	SOC.D13		
J1.18	GND				GND		
J1.19	I2C4_SDA		GPIO5_IO21	ALT5	SOC.E13		
J1.20**	ONOFF_1V8	PU 100K			SOC.A25		Run at 1.8V level!
J1.21	GND				GND		
J1.22**	PMIC_ON_REQ_1V8	PU 100K			SOC.A24		Run at 1.8V level!
J1.23	BT_HOST_WAKE						AP6275S.50
J1.24**	POR_B_1V8	4.7K			SOC.B24		Run at 1.8V level!
J1.25	WIFI_HOST_WAKE						AP6275S.16

J1.26**	PMIC_STBY_REQ_1V8	PU 100K			SOC.E24		Run at 1.8V level!
J1.27	NVCC_3V3				POWER OUT		
J1.28	SD2_RESET_B		GPIO2_IO19	ALT5	SOC.AB26		
J1.29*	SD1_DATA7		GPIO2_IO09_1v8	ALT5	SOC.W26		
J1.30	GND				GND		
J1.31	NVCC_ENET				POWER IN		
J1.32**	NAND_DATA01		GPIO3_IO07	ALT5	SOC.K24		Run at 1.8V level!
J1.33	GND				GND		
J1.34**	NAND_CE0_B		GPIO3_IO01	ALT5	SOC.N24		Run at 1.8V level!
J1.35*	CLKIN1_1V8			ALT5	SOC.H27		Run at 1.8V level!
J1.36***	NC						
J1.37*	CLKIN2_1V8		GPIO3_IO12	ALT5	SOC.J27		Run at 1.8V level!
J1.38**	NAND_DQS		GPIO3_IO14	ALT5	SOC.R22		Run at 1.8V level!
J1.39***	NC						
J1.40**	NAND_ALE		GPIO3_IO00	ALT5	SOC.N22		Run at 1.8V level!
J1.41*	GPIO1_IO07	PU1.5K	ENET_MDIO	ALT0	SOC.AF11		
J1.42***	NC		NC				
J1.43***	NC		NC				
J1.44***	NC		NC				
J1.45*	CLKOUT1_1V8			ALT5	SOC.H26		Run at 1.8V level!
J1.46**	NAND_DATA03		GPIO3_IO09	ALT5	SOC.N23		Run at 1.8V level!
J1.47*	CLKOUT2_1V8			ALT5	SOC.J26		
J1.48**	NAND_DATA00		GPIO3_IO06	ALT5	SOC.P23		Run at 1.8V level!
J1.49	GND				GND		
J1.50**	NAND_DATA02		GPIO3_IO08	ALT5	SOC.K23		Run at 1.8V level!
J1.51	PCIE1_REF_CLKM				SOC.A21		
J1.52	GND				GND		
J1.53	PCIE1_REF_CLKP				SOC.B21		
J1.54***	NC						
J1.55	GND				GND		
J1.56***	NC						
J1.57	PCIE1_TXM				SOC.A20		
J1.58	GND				GND		

J1.59	PCIE1_TXP				SOC.B20		
J1.60	PCIE1_RXM				SOC.A19		
J1.61	GND				GND		
J1.62	PCIE1_RXP				SOC.B19		
J1.63* **	NC						
J1.64	GND				GND		
J1.65* **	NC						
J1.66* **	NC						
J1.67	GND				GND		
J1.68* **	NC						
J1.69	CSI_P1_DP3				SOC.B18		
J1.70	GND				GND		
J1.71	CSI_P1_DN3				SOC.A18		
J1.72* **	NC						
J1.73	CSI_P1_DP1				SOC.B15		
J1.74	SD2_CD_B		GPIO2_IO12	ALT5	SOC.AA26		
J1.75	CSI_P1_DN1				SOC.A15		
J1.76	GND				GND		
J1.77	CSI_P1_DN2				SOC.A17		
J1.78	SD2_DATA2		GPIO2_IO17	ALT5	SOC.V24	SDIOMUX	
J1.79	CSI_P1_DP2				SOC.B17		
J1.80	SD2_DATA1		GPIO2_IO16	ALT5	SOC.AB24	SDIOMUX	
J1.81	CSI_P1_DP0				SOC.B14		
J1.82	SD2_CLK		GPIO2_IO13	ALT5	SOC.W23	SDIOMUX	
J1.83	CSI_P1_DN0				SOC.A14		
J1.84	SD2_DATA3		GPIO2_IO18	ALT5	SOC.V23	SDIOMUX	
J1.85	GND				GND		
J1.86	SD2_DATA0		GPIO2_IO15	ALT5	SOC.AB23	SDIOMUX	
J1.87	CSI_P1_CKP				SOC.B16		
J1.88	SD2_CMD		GPIO2_IO14	ALT5	SOC.W24	SDIOMUX	
J1.89	CSI_P1_CKN				SOC.A16		
J1.90	NVCC_SD2_1V8_3V3				POWER OUT		

Note:

*** Pin signals are different from TRUX-iMX8MQ SoM, see details in Section6.4**

**** Pin signaling voltage level are different from TRUX-iMX8MQ SoM, see details in Section6.4**

***** Pin signals are not connected in TRUX-iMX8MMini SoM, see details in Section6.4**

6.2 B2B J2 Pin Function List

B2B Connector Pin Number	B2B Connector Pin Name	Pull up /Pull down on SOM	i.MX 8M Mini Alternate Signals	i.MX 8M Mini Alternates	i.MX 8M Mini Ball Number	Alternate ICs Signals Name	Alternate ICs Pin Number
J2.1	JTAG_TCK			ALT5	SOC.F26		
J2.2	HPLOUT		GPIO4_IO30	ALT5	SOC.AF7	HPLOUT	WM8904.E3
J2.3	JTAG_TMS			ALT5	SOC.F27		
J2.4	HPROUT		GPIO5_IO00	ALT5	SOC.AG6	HPROUT	WM8904.E2
J2.5	JTAG_TRST_B			ALT5	SOC.C27		
J2.6	HPOUTFB		GPIO4_IO28	ALT5	SOC.AG8	HPOUTFB	WM8904.F3
J2.7	JTAG_TDI			ALT5	SOC.E27		
J2.8	LINEIN1_LP		GPIO4_IO29	ALT5	SOC.AG7	LINEIN1_LP	WM8904.A2
J2.9	JTAG_TDO			ALT5	SOC.E26		
J2.10	LINEIN1_RP		GPIO4_IO31	ALT5	SOC.AC6	LINEIN1_RP	WM8904.B2
J2.11	BOOT_MODE1			ALT5	SOC.G27		
J2.12	AGND			ALT5	AUDIO AGND		WM8904.C1
J2.13	BOOT_MODE0			ALT5	SOC.G26		
J2.14	DMIC_CLK		GPIO5_IO01	ALT5	SOC.AF6	DMIC_CLK	WM8904.A3
J2.15* **	NC						
J2.16	DMIC_DATA		GPIO5_IO02	ALT5	SOC.AD6	DMIC_DATA_1V8	WM8904.B3
J2.17* **	NC						
J2.18	GND				GND		
J2.19* **	NC						
J2.20	ECSPI2_MOSI		UART4_TXD	ALT1	SOC.B8		
J2.21* **	NC						
J2.22	ECSPI2_MISO		UART4_CTS	ALT1	SOC.A8		
J2.23	GND				GND		
J2.24	ECSPI2_SCLK		UART4_RXD	ALT1	SOC.E6		
J2.25* **	NC						
J2.26	ECSPI2_SS0		UART4_RTS	ALT1	SOC.A6		
J2.27* **	NC						
J2.28	GPIO1_IO02			ALT0	SOC.AG13		
J2.29* **	NC						
J2.30	I2C2_SDA		GPIO5_IO17		SOC.D9		
J2.31* **	NC						
J2.32	I2C2_SCL	PU 10K	GPIO5_IO16	ALT5	SOC.D10		
J2.33* **	NC						
J2.34	SAI5_RXFS		GPIO3_IO19	ALT5	SOC.AB15		
J2.35* **	NC						
J2.36	SAI5_RXD0		GPIO3_IO21	ALT5	SOC.AD18		
J2.37* **	NC						
J2.38	SAI5_RXD2		GPIO3_IO23	ALT5	SOC.AD13		

J2.39* **	NC						
J2.40	SAI5_RXC		GPIO3_IO20	ALT5	SOC.AC15		
J2.41* **	NC						
J2.42	SAI5_RXD1		GPIO3_IO22	ALT5	SOC.AC14		
J2.43* **	NC						
J2.44	SAI5_RXD3		GPIO3_IO24	ALT5	SOC.AC13		
J2.45* **	NC						
J2.46	SAI5_MCLK		GPIO3_IO25	ALT5	SOC.AD15		
J2.47	GND				GND		
J2.48	SAI2_RXFS		GPIO4_IO21	ALT5	SOC.AC19		
J2.49* **	NC						
J2.50	SAI2_RXC		GPIO4_IO22	ALT5	SOC.AB22		
J2.51* **	NC						
J2.52	SAI2_TXFS		GPIO4_IO24	ALT5	SOC. AD23		
J2.53	GND				GND		
J2.54	SAI2_MCLK		GPIO4_IO27	ALT5	SOC.AD19		
J2.55	SAI1_RXFS		GPIO4_IO00	ALT5	SOC.AG16		
J2.56	SAI2_TXC		GPIO4_IO25	ALT5	SOC.AD22		
J2.57	SAI1_RXC		GPIO4_IO01	ALT5	SOC.AF16		
J2.58	SAI2_RXD0		GPIO4_IO23	ALT5	SOC.AC24		
J2.59	SAI1_RXD1	PU 10K	BOOT_CFG01	ALT6	SOC.AF15		
J2.60	SAI2_TXD0		GPIO4_IO26	ALT5	SOC.AC22		
J2.61	SAI1_RXD0		BOOT_CFG00	ALT6	SOC.AG15		
J2.62	SAI1_RXD3		BOOT_CFG03	ALT6	SOC.AF17		
J2.63	SAI1_RXD2	PU 10K	BOOT_CFG02	ALT6	SOC.AG17		
J2.64	SAI1_TXFS		GPIO4_IO10	ALT5	SOC.AB19		
J2.65	SAI1_RXD4		BOOT_CFG04	ALT6	SOC.AG18		
J2.66	SAI1_RXD6	PU 10K	BOOT_CFG06	ALT6	SOC.AG19		
J2.67	SAI1_TXD1		BOOT_CFG09	ALT6	SOC.AF20		
J2.68	SAI1_RXD7		BOOT_CFG07	ALT6	SOC.AF19		
J2.69	SAI1_RXD5	PU 10K	BOOT_CFG05	ALT6	SOC.AF18		
J2.70	SAI1_TXD0		BOOT_CFG08	ALT6	SOC.AG20		
J2.71	SAI1_TXD5	PU 10K	BOOT_CFG13	ALT6	SOC.AF22		
J2.72	SAI1_TXC		GPIO4_IO11	ALT5	SOC.AC18		
J2.73	SAI1_TXD3	PU 10K	BOOT_CFG11	ALT6	SOC.AF21		
J2.74	SAI1_TXD4		BOOT_CFG12	ALT6	SOC.AG22		
J2.75	GND				GND		
J2.76	SAI1_TXD7		BOOT_CFG15	ALT6	SOC.AF23		
J2.77	ECSPI1_SCLK		GPIO5_IO06	ALT5	SOC.D6		
J2.78	SAI1_TXD2		BOOT_CFG10	ALT6	SOC.AG21		
J2.79	ECSPI1_SS0		GPIO5_IO09	ALT5	SOC.B6		
J2.80	SAI1_TXD6		BOOT_CFG14	ALT6	SOC.AG23		
J2.81	ECSPI1_MISO		GPIO5_IO08	ALT5	SOC.A7		
J2.82	SAI1_MCLK		GPIO4_IO20	ALT5	SOC.AB18		
J2.83	ECSPI1_MOSI		GPIO5_IO07	ALT5	SOC.B7		

J2.84	GND				GND		
J2.85	UART2_RXD		GPIO5_IO24	ALT5	SOC.F15		
J2.86	UART2_TXD		GPIO5_IO25	ALT5	SOC.E15		
J2.87	UART3_RXD		GPIO5_IO26	ALT5	SOC.E18		
J2.88	UART1_RXD		GPIO5_IO22	ALT5	SOC.E14		
J2.89	UART3_TXD		GPIO5_IO27	ALT5	SOC.D18		
J2.90	UART1_TXD		GPIO5_IO23	ALT5	SOC.F13		

Note:
***** Pin signals are not connected in TRUX- iMX8MMini SoM. But they are connected in TRUX- iMX8MQ SoM for HDMI signals.**

6.3 B2B J3 Pin Function List

B2B Connector Pin Number	B2B Connector Pin Name	Pull up /Pull down on SOM	i.MX 8M Mini Alternate Signals	i.MX 8M Mini Alternates	i.MX 8M Mini Ball Number	Alternate ICs Signals Name	Alternate ICs Pin Number
J3.1	GPIO5_IO29		UART4_TXD	ALT0	SOC.F18		
J3.2	NC						
J3.3	GPIO5_IO28		UART4_RXD	ALT0	SOC.F19		
J3.4	NC						
J3.5	NC						
J3.6	NC						
J3.7	NC						
J3.8	NC						
J3.9	GND				GND		
J3.10	GND				GND		
J3.11	NC						
J3.12	MIPI_DSI_TX0_P				SOC.B9		
J3.13	NC						
J3.14	MIPI_DSI_TX0_N				SOC.A9		
J3.15	GND				GND		
J3.16	MIPI_DSI_TX1_P				SOC.B10		
J3.17	NC						
J3.18	MIPI_DSI_TX1_N				SOC.A10		
J3.19	NC						
J3.20	MIPI_DSI_TX3_P				SOC.B13		

J3.21	GND				GND		
J3.22	MIPI_DSI_TX3_N				SOC.A13		
J3.23	MIPI_DSI_TX2_P				SOC.B12		
J3.24	GND				GND		
J3.25	MIPI_DSI_TX2_N				SOC.A12		
J3.26	USB2_VBUS				SOC.F23		
J3.27	GND				GND		
J3.28	SPDIF_RX		GPIO5_IO04	ALT2	SOC.AG9		
J3.29	MIPI_DSI_CLK_N				SOC.A11		
J3.30	GPIO1_IO11				SOC.AC10		
J3.31	MIPI_DSI_CLK_P				SOC.B11		
J3.32	SPDIF_EXT_CLK		GPIO5_IO05	ALT2	SOC.AF8		FXL4TD245 UMX.11
J3.33	GND				GND		
J3.34	GND				GND		
J3.35* **	NC						
J3.36	SPDIF_TX		GPIO5_IO03	ALT2	SOC.AF9		
J3.37* **	NC						
J3.38	GPIO1_IO15				SOC.AB9		
J3.39	GND						
J3.40	GPIO1_IO13				SOC.AD9		
J3.41* **	NC						
J3.42	I2C3_SDA		GPIO5_IO19	ALT3	SOC.F10		
J3.43* **	NC						
J3.44	USB2_ID				SOC.D23		
J3.45	GND						
J3.46	I2C3_SCL		GPIO5_IO18	ALT3	SOC.E10		
J3.47	USB2_DP				SOC.B23		
J3.48	GPIO1_IO14				SOC.AC9		
J3.49	USB2_DN				SOC.A23		
J3.50	GPIO1_IO12				SOC.AB10		
J3.51	GND						
J3.52	GPIO1_IO10				SOC.AD10		
J3.53* **	NC						

J3.54	GPIO1_IO03				SOC.AF13		
J3.55* **	NC						
J3.56	USB1_ID				SOC.D22		
J3.57	GND						
J3.58	GPIO1_IO06				SOC.AG11		
J3.59* **	NC						
J3.60	GPIO1_IO08				SOC.AG10		
J3.61* **	NC						
J3.62	GPIO1_IO05				SOC. AF12		
J3.63	GND				GND		
J3.64	GPIO1_IO01				SOC. AF14		
J3.65	USB1_DP				SOC.B22		
J3.66	USB1_VBUS				SOC.F22		
J3.67	USB1_DN				SOC.A22		
J3.68	GND				GND		
J3.69* **	NC						
J3.70* **	NC						
J3.71	VBAT				POWER IN		
J3.72* **	NC						
J3.73	VBAT				POWER IN		
J3.74	GND				GND		
J3.75	VBAT				POWER IN		
J3.76* **	NC						
J3.77	VBAT				POWER IN		
J3.78* **	NC						
J3.79	VBAT				POWER IN		
J3.80* **	NC						
J3.81	VBAT				POWER IN		
J3.82* **	NC						
J3.83	VBAT				POWER IN		
J3.84* **	NC						
J3.85	VBAT				POWER IN		
J3.86* **	NC						

J3.87	VBAT				POWER IN		
J3.88* **	NC						
J3.89	VBAT				POWER IN		
J3.90* **	NC						

Note:
***** Pin signals are not connected in TRUX- iMX8MMini SoM. But they are connected in TRUX- iMX8MQ SoM for USB 3.0 TX/RX and MIPI CSI-2 signals.**

Supply Pin Description: -

B2B Pin Number	B2B Connector Pin Name	Remarks
J1.27	NVCC_3V3	Max 100mA
J1.90	NVCC_SD2_1V8_3V3	SOM IO power for the SD2 interface SD2 signals can be pulled to NVCC_SD2_1V8_3V3
J1.15	NVCC_SNVS_1V8	SOM power for NVCC_SNVS
J3(71,73,75,77,79,81,83,85,87,89)	VBAT	Input supply to SOM from Carrier board

6.4 B2B Pinout comparison for TRUX-iMX8MMini-Q01 and TRUX-iMX8MQ-Q01

B2B Pin Number	TRUX-iMX8MMini-Q01 Pin name	TRUX-iMX8MQ-Q01 Pin name	Remarks
J1.29	GPIO2_IO09_1V8	SD2_WP	Note: * Pin signals changed. These signals are different from TRUX-iMX8MQ
J1.35	CLKIN1_1V8	NAND_DATA07	
J1.37	CLKIN2_1V8	NAND_DATA06	
J1.41	GPIO1_IO07	NAND_RE_B	
J1.45	CLKOUT1_1V8	NAND_CLE	
J1.47	CLKOUT2_1V8	NAND_CE2_B	
J1.15	NVCC_SNVS_1V8 [1V8]	NVCC_SNVS [3V3]	Note: ** Voltage level changed. These signals are at different voltage from TRUX-iMX8MQ
J1.20	ONOFF_1V8 [1V8]	ONOFF [3V3]	
J1.22	PMIC_ON_REQ_1V8 [1V8]	PMIC_ON_REQ [3V3]	
J1.24	POR_B_1V8 [1V8]	POR_B [3V3]	
J1.26	PMIC_STBY_REQ_1V8 [1V8]	PMIC_STBY_REQ [3V3]	
J1.32	NAND_DATA01 [1V8]	NAND_DATA01 [3V3]	
J1.34	NAND_CE0_B [1V8]	NAND_CE0_B [3V3]	
J1.38	NAND_DQS [1V8]	NAND_DQS [3V3]	
J1.40	NAND_ALE [1V8]	NAND_ALE [3V3]	
J1.46	NAND_DATA03 [1V8]	NAND_DATA03 [3V3]	

J1.48	NAND_DATA00 [1V8]	NAND_DATA00 [3V3]	
J1.50	NAND_DATA02 [1V8]	NAND_DATA02 [3V3]	
J1.36	NC	NAND_READY_B	Note: *** Not Connected. These pins are not connected in TRUX-iMX8MMini SoM
J1.39	NC	NAND_DATA04	
J1.42	NC	NAND_WP_B	
J1.43	NC	NAND_DATA05	
J1.44	NC	NAND_WE_B	
J1.54	NC	PCIE2_REF_CLKN	
J1.56	NC	PCIE2_REF_CLKP	
J1.63	NC	PCIE2_RXN	
J1.65	NC	PCIE2_RXP	
J1.66	NC	PCIE2_TXN	
J1.68	NC	PCIE2_TXP	
J1.72	NC	EN_VBAT_3V3	

7. Boot Mode Configuration

The chip will always boot from the A53 core first, the M4 core will be held in reset during the A53 boot and won't run until it is enabled by the A53 core. The image for the M4 core will be loaded into memory and authenticated by the A53 core. The resistor setting is used to select the interface for booting.

TRUX-iMX8MMini-Q01 SOM supports two boot mode signals on B2B Connector. BOOT_MODE is initialized by sampling the BOOT_MODE0 and BOOT_MODE1 inputs on the rising B2B of POR_B. These Boot mode selection signals are connected to B2B connector and desired boot mode must be set from the carrier board as explained in the below table.

Signal	J2 B2B Pin number	I/O	Description
BOOT_MODE0	13	I	Used to set Mode of boot
BOOT_MODE1	11	I	Used to set Mode of boot

Booting Configuration through SD Card / eMMC:

Signal	B2B Pin number	Description
BOOT_CONFIG0	J2.61	All boot configuration pins are MUX GPIOs
BOOT_CONFIG1	J2.59	
BOOT_CONFIG2	J2.63	
BOOT_CONFIG3	J2.62	
BOOT_CONFIG4	J2.65	
BOOT_CONFIG5	J2.69	
BOOT_CONFIG6	J2.66	
BOOT_CONFIG7	J2.68	
BOOT_CONFIG8	J2.70	
BOOT_CONFIG9	J2.67	
BOOT_CONFIG10	J2.78	
BOOT_CONFIG11	J2.73	
BOOT_CONFIG12	J2.74	
BOOT_CONFIG13	J2.71	
BOOT_CONFIG14	J2.80	
BOOT_CONFIG15	J2.76	

8. Connectivity

8.1 10/100/1000 Mbps Ethernet PHY

The TRUX-iMX8MMini-Q01 features Realtek RTL8211FSI Integrated Ethernet PHY. The RTL8211FSI Ethernet transceiver requires only a single 1.8V power supply.

The RTL8211FSI Ethernet PHY supports IEEE 802.3ab/u/az-2010 standard. The key features include:

- 10BASE-T/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- Supports RGMII with 3.3/2.5/1.8/1.5V signal voltage.
- Supports crossover detection & auto-correction.
- Supports PCS and auto-negotiation with next page support.
- Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up.
- Robust operation over up to 120 meters of CAT5 cable

8.2 Ethernet Controller

The Ethernet MAC in i.MX 8M Mini CPU is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. It is connected to a B2B connector which works at 3.3V, 2.5V and 1.8V IO voltage level. The module has dedicated hardware to support the IEEE 1588 standard.

Ethernet MAC controller supports IEEE 802.3az standard.
The key features include:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking.
- Dynamically configurable to support 10/100-Mbit/s and gigabit operation.
- Seamless interface to commercial Ethernet PHY devices via one of the following:
- 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz
- 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz
- 2-bit Reduced MII (RMII) operating at 50 MHz (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz
- Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only.

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J1.4	ETH_TRX1_N	O	ENET RGMII Transmit Data 0	SOC.AG26
J1.2	ETH_TRX1_P	O	ENET RGMII Transmit Data 1	SOC.AF26
J1.6	ETH_TRX0_N	O	ENET RGMII Transmit Data 2	SOC.AG25
J1.8	ETH_TRX0_P	O	ENET RGMII Transmit Data 3	SOC.AF25
J1.5	LED_LINK10_100	O	ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AG24
J1.3	ENET_TX_CTL_OUT	O	ENET RGMII Transmit data Control	SOC.AF24

J1.10	ETH_TRX2_P	I	ENET RGMII Receive Data 0	SOC.AE27
J1.12	ETH_TRX2_N	I	ENET RGMII Receive Data 1	SOC.AD27
J1.14	ETH_TRX3_P	I	ENET RGMII Receive Data 2	SOC.AD26
J1.16	ETH_TRX3_N	I	ENET RGMII Receive Data 3	SOC.AC26
J1.7	LED_LINK1000	I	ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD [3:0] and RX_CTL	SOC.AE26
J1.9	LED_ACT	I	ENET RGMII Receive data Control	SOC.AF27
J1.13	ENET_MDC_OUT	O	RGMII Interface	SOC.AC27
J1.11	ENET_MDIO_OUT	IO	RGMII Interface	SOC.AB27
J2.32	I2C2_SCL	I	IEEE1588 Interface	SOC.D10
J2.30	ENET1_1588_EVENT1_OUT	O	IEEE1588 Interface	SOC.D9
J1.1	ENET_PHY_REF_CLK_ROOT	O	IEEE1588 Interface	SOC.AG14

8.3 Wi-Fi & BT & SD/SDIO

The WiFi/BT (AP6275S) module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface. The modules also provide a Bluetooth/BLE platform through the UART HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11ax/ac/a/b/g/n 2x2 WiFi with Bluetooth5.0 Combo Sip Module
- Two U.FL2 JACK connector for external antenna (**Part number used on SoM: Hirose; U. FL-R-SMT-1(60)**)
- **Antenna cable connected to module must have 50-Ω impedance**
- Latest Linux and Android drivers supported
- Wi-Fi/BT module broad country certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)

Bluetooth Interface

Bluetooth interface with UART4 (RXD, TXD, CTS and RTS) controlled using tristate buffer. Will allow isolation from the WiFi/BT module and the use by external circuitry via the TRUX-iMX8MMini-Q01 connector.

WIFI/SD Interface

WiFi and SD interface are provided from i.MX 8M Mini CPU. WIFI / BT (SDIO1 interface) connected via buffer and SD card (SDIO2 interface) signals given on B2B connector.

9. Peripheral Description

9.1 UART Interface

TRUX-iMX8MMini-Q01 SOM supports four UART interface on B2B connector in which one is for Debug UART interface and other two are for Data interface. i.MX 8M Mini CPU's UART1 controller is used for Debug UART interface and UART2 & UART3 controller is used for Data UART interface on B2B connector without hardware flow control. UART4 is used for BT interface.
For UART signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J2.90	UART1_TXD	O	UART1 Transmit Data	SOC.F13
J2.88	UART1_RXD	I	UART1 Receive Data	SOC.E14
J2.86	UART2_TXD	O	UART2 Transmit Data	SOC.E15
J2.85	UART2_RXD	I	UART2 Receive Data	SOC.F15
J2.89	UART3_TXD	O	UART3 Transmit Data	SOC.D18
J2.87	UART3_RXD	I	UART3 Receive Data	SOC.E18
J2.20	UART4_TXD	O	UART4 Transmit Data	SOC.B8
J2.24	UART4_RXD	I	UART4 Receive Data	SOC.E6
J2.26	UART4_RTS	I	UART4 Ready to Send	SOC.A6
J2.22	UART4_CTS	O	UART4 Clear To Send	SOC.A8

9.2 SD Interface

TRUX-iMX8MMini-Q01 SOM supports one SD card interface. i.MX 8M Mini CPU's uSDHC2 controller is used for SD interface which is fully compliant with SD Memory Card Specifications v3.0 including extended-capacity SDHC cards.
For SD Card signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J1.74	SD2_nCD	I	SD2 Card detect	SOC.AA26
J1.86	SD2_DATA0	IO	SD2 interface data 0 signal	SOC.AB23
J1.80	SD2_DATA1	IO	SD2 interface data 1 signal	SOC.AB24
J1.78	SD2_DATA2	IO	SD2 interface data 2 signal	SOC.V24
J1.84	SD2_DATA3	IO	SD2 interface data 3 signal	SOC.V23

J1.88	SD2_CMD	IO	SD2 interface command signal	SOC.W24

9.3 Display Interface

TRUX-iMX8MMini-Q01 SOM features one MIPI DSI serial port, operating up to a maximum bit rate of 1.5 Gbps. All four lanes are used for interfacing. This module provides i.MX 8M Mini CPU's MIPI DSI controller with four-lane MIPI display serial interface.
For MIPI DSI signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J3.29	DSI_CKN	MIPI DSI	MIPI D-PHY Clock Negative	SOC.A11
J3.31	DSI_CKP	MIPI DSI	MIPI D-PHY Clock Positive	SOC.B11
J3.12	DSI_DP0	MIPI DSI	MIPI D-PHY LANE0 Positive	SOC.B9
J3.14	DSI_DN0	MIPI DSI	MIPI D-PHY LANE0 Negative	SOC.A9
J3.16	DSI_DP1	MIPI DSI	MIPI D-PHY LANE1 Positive	SOC.B10
J3.18	DSI_DN1	MIPI DSI	MIPI D-PHY LANE1 Negative	SOC.A10
J3.23	DSI_DP2	MIPI DSI	MIPI D-PHY LANE2 Positive	SOC.B12
J3.25	DSI_DN2	MIPI DSI	MIPI D-PHY LANE2 Negative	SOC.A12
J3.20	DSI_DP3	MIPI DSI	MIPI D-PHY LANE3 Positive	SOC.B13
J3.22	DSI_DN3	MIPI DSI	MIPI D-PHY LANE3 Negative	SOC.A13

9.4 Camera Interface

This module provides one four-lane MIPI camera serial interface. It operate up to a maximum bit rate of 1.5 Gbps. All four lanes are used for interfacing. The i.MX 8M Mini incorporates the MIPI CSI Host Controller.
For MIPI CSI signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J1.89	CSI_P1_CKN	MIPI CSI	MIPI-CSI Port 1 Clock Negative	SOC.A16
J1.87	CSI_P1_CKP	MIPI CSI	MIPI-CSI Port 1 Clock Positive	SOC.B16
J1.83	CSI_P1_DN0	MIPI CSI	MIPI-CSI Port 1 Data 0 Negative	SOC.A14
J1.81	CSI_P1_DP0	MIPI CSI	MIPI-CSI Port 1 Data 0 Positive	SOC.B14
J1.75	CSI_P1_DN1	MIPI CSI	MIPI-CSI Port 1 Data 1 Negative	SOC.A15

J1.73	CSI_P1_DP1	MIPI CSI	MIPI-CSI Port 1 Data 1 Positive	SOC.B15
J1.77	CSI_P1_DN2	MIPI CSI	MIPI-CSI Port 1 Data 2 Negative	SOC.A17
J1.79	CSI_P1_DP2	MIPI CSI	MIPI-CSI Port 1 Data 2 Positive	SOC.B17
J1.71	CSI_P1_DN3	MIPI CSI	MIPI-CSI Port 1 Data 3 Negative	SOC.A18
J1.69	CSI_P1_DP3	MIPI CSI	MIPI-CSI Port 1 Data 3 Positive	SOC.B18

9.5 I2C Interface

TRUX-iMX8MMini-Q01 SOM features three I2C interface on B2B connector. i.MX 8M Mini CPU's I2C2, I2C3, I2C4 channel is used for General purpose I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. I2C1 is connected to PMIC on SOM.
For I2C signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J2.32	I2C2_SCL	IO	I2C2 clock	SOC.D10
J2.30	I2C2_SDA	IO	I2C2 data	SOC.D9
J3.46	I2C3_SCL	IO	I2C3 clock	SOC.E10
J3.42	I2C3_SDA	IO	I2C3 data	SOC.F10
J1.17	I2C4_SCL	IO	I2C4 clock	SOC.D13
J1.19	I2C4_SDA	IO	I2C4 data	SOC.E13

9.6 PWM Interface

TRUX-iMX8MMini-Q01 SOM features four PWM interfaces on B2B connector. i.MX 8M Mini CPU's PWM1, PWM2, PWM3 and PWM4 module is used for PWM interface. The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO.
For PWM signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J3.64	GPIO1_IO01	O	Pulse Width Modulation 1	SOC.AF14
J3.40	GPIO1_IO13	O	Pulse Width Modulation 2	SOC.AD9
J3.48	GPIO1_IO14	O	Pulse Width Modulation 3	SOC.AC9

J3.38	GPIO1_IO15	O	Pulse Width Modulation 4	SOC.AB9

9.7 GPIO Interface

GPIO Interface is used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O. Most of the i.MX 8M Mini CPU Pins which are connected to B2B connector can be configured as GPIO. i.MX 8M Mini CPU GPIO controller provides dedicated general-purpose pins that can be configured as either inputs or outputs.

For GPIO signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Pad	Mode	Ball no.
J1.1	GPIO1_IO00	REF_CLK_32K	ALT2	SOC.AG14
J1.29	GPIO2_IO09_1V8	SD1_DATA7	ALT0	SOC.W26
J1.41	GPIO1_IO07	ENET_MDIO	ALT0	SOC.AF11
J3.1	GPIO5_IO29	UART4_TXD	ALT0	SOC.F18
J3.3	GPIO5_IO28	UART4_RXD	ALT0	SOC.F19
J3.30	GPIO1_IO11	USB2_OTG_ID	ALT1	SOC.AC10
J3.38	GPIO1_IO15	USB2_OTG_OC	ALT1	SOC.AB9
J3.40	GPIO1_IO13	USB1_OTG_OC	ALT1	SOC.AD9
J3.48	GPIO1_IO14	USB2_OTG_PWR	ALT1	SOC.AC9
J3.50	GPIO1_IO12	USB1_OTG_PWR	ALT1	SOC.AB10
J3.52	GPIO1_IO10	USB1_OTG_ID	ALT1	SOC.AD10
J3.54	GPIO1_IO03	USDHC1_VSELECT	ALT1	SOC.AF13
J3.58	GPIO1_IO06	USDHC1_CD	ALT1	SOC.AG11
J3.62	GPIO1_IO05	PMIC_READY	ALT2	SOC.AF12
J3.64	GPIO1_IO01	CCM_EXT_CLK2	ALT3	SOC.AF14

9.8 USB 2.0

TRUX-iMX8MMini-Q01 SOM features two High Speed USB 2.0 OTG interfaces (USB1 & USB2) on B2B connector. i.MX 8M Mini CPU's USB Controller which has two independent USB On-The-Go (OTG) controller cores are used for USB OTG interface.
For USB 2.0 signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J3.65	USB1_DP	DSIO	USB PHY 2.0 Data Positive	SOC.B22
J3.67	USB1_DN	DSIO	USB PHY 2.0 Data Negative	SOC.A22
J3.47	USB2_DP	DSIO	USB PHY 2.0 Data Positive	SOC.B23
J3.49	USB2_DN	DSIO	USB PHY 2.0 Data Negative	SOC.A23

9.9 PCI Express (Gen 2.0)

TRUX-iMX8MMini-Q01 SOM exposes one, PCI Express GEN 2 single lane interfaces. PCI Express port requires an external 100MHz PCIe compliant reference clock.
For PCI Express signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J1. 51	PCIE1_REF_CLKM	DSI	PCIE compliant 100MHz reference clock Negative	SOC.A21
J1.53	PCIE1_REF_CLKP	DSI	PCIE compliant 100MHz reference clock Positive	SOC.B21
J1.57	PCIE1_TXM	DSO	PCIE GEN2.1 Transmit Data Negative	SOC.A20
J1.59	PCIE1_TXP	DSO	PCIE GEN2.1 Transmit Data Positive	SOC.B20
J1.60	PCIE1_RXM	DSI	PCIE GEN2.1 Receive Data Negative	SOC.A19
J1.62	PCIE1_RXP	DSI	PCIE GEN2.1 Receive Data Positive	SOC.B19

9.10 QSPI

TRUX-iMX8MMini-Q01 SOM features QSPI interface on B2B connector, which can be used to interface external serial flash devices. For QSPI signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J1.48	QSPIA_DATA0_1V8	IO	Flash Data I/O 0	SOC.P23
J1.32	QSPIA _DATA1_1V8	IO	Flash Data I/O 1	SOC.K24
J1.50	QSPIA _DATA2_1V8	IO	Flash Data I/O 2	SOC.K23
J1.46	QSPIA _DATA3_1V8	IO	Flash Data I/O 3	SOC.N23
J1.34	QSPIA _ SS0_B_1V8	O	Chip Enable 0	SOC.N24
J1.38	QSPIA _ DQS_1V8	I/O	Flash Data strobe signal	SOC.R22
J1.40	QSPIA _ SCLK_1V8	O	Flash Serial Clock	SOC. N22

9.11 Digital Audio serial interface: I2S (SAI), S/PDIF

TRUX-iMX8MMini-Q01 SOM features four SAI interfaces (SAI1, SAI2, SAI3 & SAI5) and one SPDIF on B2B connector. i.MX 8M Mini CPU's SAI modules are used for SAI interface. For more details, refer B2B connector J2.

For SAI and S/PDIF signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J2.82	SAI1_MCLK	I	SAI1 Audio Master Clock	SOC.AB18
J2.64	SAI1_TXFS	I/O	SAI1 Transmit Frame Sync.	SOC.AB19
J2.72	SAI1_TXC	I/O	SAI1 Transmit Bit Clock	SOC.AC18
J2.70	SAI1_TXD0	O	SAI1 Transmit Data 0	SOC.AG20
J2.67	SAI1_TXD1	O	SAI1 Transmit Data 1	SOC.AF20
J2.78	SAI1_TXD2	O	SAI1 Transmit Data 2	SOC.AG21
J2.73	SAI1_TXD3	O	SAI1 Transmit Data 3	SOC.AF21
J2.74	SAI1_TXD4	O	SAI1 Transmit Data 4	SOC.AG22
J2.71	SAI1_TXD5	O	SAI1 Transmit Data 5	SOC.AF22
J2.80	SAI1_TXD6	O	SAI1 Transmit Data 6	SOC.AG23
J2.76	SAI1_TXD7	O	SAI1 Transmit Data 7	SOC.AF23
J2.55	SAI1_RXFS	I/O	SAI1 Receive Frame Sync.	SOC.AG16

J2.57	SAI1_RXC	I/O	SAI1 Receive Bit Clock	SOC.AF16
J2.61	SAI1_RXD0	I	SAI1 Receive Data 0	SOC.AG15
J2.59	SAI1_RXD1	I	SAI1 Receive Data 1	SOC.AF15
J2.63	SAI1_RXD2	I	SAI1 Receive Data 2	SOC.AG17
J2.62	SAI1_RXD3	I	SAI1 Receive Data 3	SOC.AF17
J2.65	SAI1_RXD4	I	SAI1 Receive Data 4	SOC.AG18
J2.69	SAI1_RXD5	I	SAI1 Receive Data 5	SOC.AF18
J2.66	SAI1_RXD6	I	SAI1 Receive Data 6	SOC.AG19
J2.68	SAI1_RXD7	I	SAI1 Receive Data 7	SOC.AF19
J2.54	SAI2_MCLK	I	SAI2 Audio Master Clock	SOC.AD19
J2.52	SAI2_TXFS	I/O	SAI2 Transmit Frame Sync.	SOC.AD23
J2.56	SAI2_TXC	I/O	SAI2 Transmit Bit Clock	SOC.AD22
J2.60	SAI2_TXD	O	SAI2 Transmit Data	SOC.AC22
J2.48	SAI2_RXFS	I/O	SAI2 Receive Frame Sync.	SOC.AC19
J2.50	SAI2_RXC	I/O	SAI2 Receive Bit Clock	SOC.AB22
J2.58	SAI2_RXD	I	SAI2 Receive Data	SOC.AC24
J2.46	SAI5_MCLK	I	SAI5 Audio Master Clock	SOC.AD15
J2.34	SAI5_RXFS	I/O	SAI5 Receive Frame Sync.	SOC.AB15
J2.40	SAI5_RXC	I/O	SAI5 Receive Bit Clock	SOC.AC15
J2.36	SAI5_RXD0	I	SAI5 Receive Data 0	SOC.AD18
J2.42	SAI5_RXD1	I	SAI5 Receive Data 1	SOC.AC14
J2.38	SAI5_RXD2	I	SAI5 Receive Data 2	SOC.AD13
J2.44	SAI5_RXD3	I	SAI5 Receive Data 3	SOC.AC13
J3.28	SPDIF_RX	I	SPDIF Receive data	SOC.AG9
J3.32	SPDIF_EXT_CLK	I	SPDIF External Clock	SOC.AF8
J3.36	SPDIF_TX	O	SPDIF Transmit data	SOC.AF9

9.12 ECSPI Enhanced Configurable SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s. For ECSPI signal details, refer below table:-

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description	Ball no.
J2.83	ECSPI1_MOSI	I/O	SPI Master data Out - Slave data In signal	SOC.B7
J2.81	ECSPI1_MISO	I/O	SPI Master data In - Slave data Out signal	SOC.A7
J2.77	ECSPI1_SCLK	O	SPI Serial Clock	SOC.D6
J2.79	ECSPI1_SS0	O	SPI Slave Select Signal	SOC.B6

10. Electrical Characteristics

10.1 Power Signal

TRUX-iMX8MMini-Q01 SOM works with 3.5V – 5V power input (VBAT) from B2B connector and generates all other required powers using PMIC internally on SOM itself. SOM uses VBAT power input from J3 B2B connector to PMIC and then generates various power rails for i.MX 8M Mini CPU.

B2B connector Pin number	Signal	Signal Type	Description
J3.71, 73, 75, 77, 79, 81, 83, 85, 87, 89	VBAT	I	Input to SOM
J1.15	NVCC_SNVS_1V8	O	SNVS Domain power rail input
J1.27	NVCC_3V3	O	SOM Peripherals 3.3V Output
J1.90	NVCC_SD2_1V8_3V3	O	SOM IO power for the SD2 interface
J3.26	USB2_VBUS	I	USB2 PHY VBUS - 5V tolerant
J3.66	USB1_VBUS	I	USB1 PHY VBUS - 5V tolerant
J1.31	NVCC_ENET	I or O	SOC ENET domain power is 1.8V Note: 1. SOM configuration with PHY, can be left floating or ground with 1uF capacitor. SOM configuration without PHY, must connect 1.8/2.5/3.3V supply input
J1.18,21,30 ,33,49,52 ,55,58,61 ,64,67,70 ,76,85	GND	GND	J1 Digital Ground
J2. 18,23,47, 53,75,84	GND	GND	J2 Digital Ground
J3. 9,10,15, 21,24,27, 33,34,39, 45,51,57, 63,68,74	GND	GND	J3 Digital Ground
J2.12	AGND	AGND	Audio GND

10.2 Power Requirement

Power Signal	Min (V)	Typical (V)	Max (V)
VBAT	3.5	3.7	5
NVCC_SNVS_1V8	1.7	1.8	1.9
USB1_VBUS	4.5	5	5.25
USB2_VBUS	4.5	5	5.25

10.3 Power Consumption

Mode	Voltage	Nominal Current	Peak current	Power @ nominal current	Conditions
Run	3.35V	0.68A	1.021A	2.281W	Linux up

Run	3.35V	0.58A	0.876A	1.956W	Linux up, Wi-Fi connected and Iperf is running
4K video playback	3.35V	0.42A	0.633A	1.413W	Linux up, Wi-Fi connected and 3840x2160@30Hz
FHD video playback	3.35V	0.42A	0.637A	1.423W	Linux up, Wi-Fi connected and 1920x1080@60Hz
Standby	3.4V	15mA	22.5mA	51mW	Memory retention mode
Off	3.35V	300uA	450uA	1mW	All power rails are Off, only Internal SOC RTC is powered

Note: The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing as per their specific operation scenarios.

10.4 Control Signals

B2B Connector Pin Number	B2B Connector Pin Name	Signal Type	Signal Description
J1.20	ONOFF	I	Input to SoC; Internal PU on SoM to NVCC_SNVS_1V8. When pulled 5 second or more to GND, SOM SoC will be ON or OFF
J1.24	POR_B	I/O	OD output from PMIC; Internal PU on SOM to NVCC_SNVS_1V8. Can be used to generate SoC Reset without power cycle.
J1.26	PMIC_STBY_REQ	O	Output from SoC & input to PMIC; Internal PU on SOM to NVCC_SNVS_1V8. 0 to 1: Enter Standby 1 to 0: Wake up from standby
J1.22	PMIC_ON_REQ	O	Output from SoC & input to PMIC; Internal PU on SOM to VBAT
J1.23	BT_HOST_WAKE	O	Output from Bluetooth to wake Host (1.8V signal)
J1.25	WIFI_HOST_WAKE	O	Output from Bluetooth to wake Host (1.8V signal)
J1.1	GPIO1_IO00(32.768KHz)	O	Used internally in SOM as 32.768Khz reference clock
J2.28	GPIO1_IO02(WDOG_B)	O	Used internally in SOM as watchdog reset
J3.60	GPIO1_IO08	O	Used internally in SOM with "WIFI/BT" Configuration
J3.62	GPIO1_IO05	O	Used internally in SOM with "WIFI/BT" Configuration

10.5 Reset

TRUX-iMX8MMini-Q01 SOM features reset signals from carrier board by using push button switch. These signals are connected from J1 B2B connector to i.MX 8M CPU's pins. This allows resetting the SOM through push button on carrier board.

Signal	B2B connector Pin number
POR_B	J1.24
ONOFF	J1.20
PMIC_STBY_REQ	J1.26
PMIC_ON_REQ	J1.22

11. Mechanical Dimensions

11.1 TRUX-iMX8MMini-Q01 SoM Dimensions

TRUX-iMX8MMini-Q01 SOM has 55.1mm x 30.2mm x 5.00mm (Carrier PCB to highest component on SOM) size as shown below:

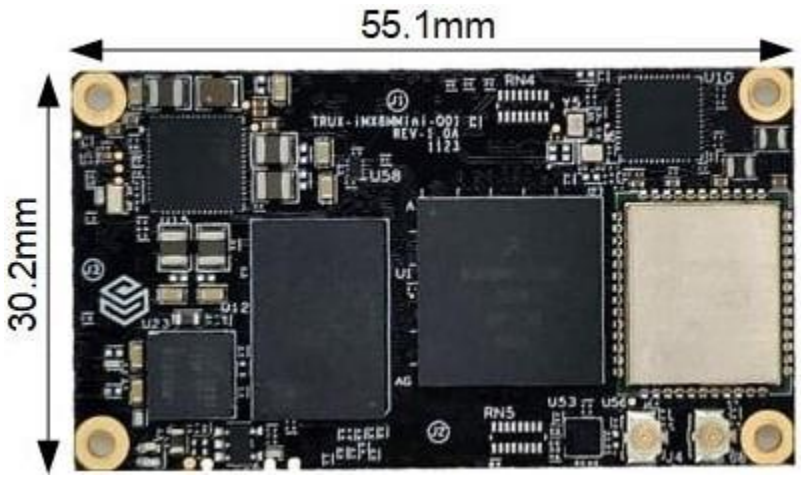


Figure4: Mechanical dimensions of TRUX-iMX8MMini-Q01 SOM

11.2 Carrier Board Mounting

TRUX-iMX8MMini-Q01 SOM has four mounting holes (M2) for mounting it to the carrier board which are plated holes and connected to GND.

90-pin board-to-board connectors **Hirose P/N: DF40C-90DP-0.4V(51)** are different from mating carrier board 90-pin connectors.

11.3 Standoff and Screw

For mounting in harsh vibration environments can use the following standoff:

Standoff: **Wurth elektronik; 9774015243R**

Screw: **MiSUMi; CBSTSE2-3**

NOTE: The M2 screws head diameter must be smaller than 4mm.

11.4 Thermal Management

Full operation scenarios may prompt the use of an external heat dissipation solution.

The implemented solution design may vary depending on the device operation scenario as well as its mechanical design.

The following solution was implemented in the TRUX-iMX8MMini-Q01 evaluation kits.

Heat sink P/N: TRUX-HS-SOM-Q01 with an embedded double-sided adhesive mounted on SOM.

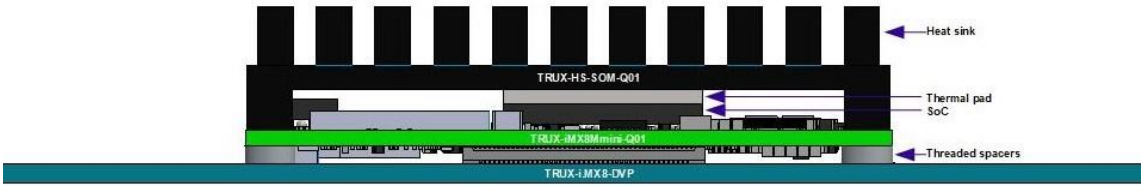


Figure5: Stack arrangement of TRUX-iMX8-DVP, TRUX-iMX8MMini-Q01 SOM and heat sink

Figure6: Heat sink image of TRUX-iMX8MMini-Q01

Thermal conductive gap filler with similar performance to " TIF™700 Series Thermally Gap Filler "; with appropriate thickness P/N: TIF760P (1.5mm)

Screw for heatsink mounting: M2 x 0.4mm Length 12mm

NOTE: The heat gap filler will allow a moderate heat generation on the SOM board to dissipate through the carrier board. In this case, it is recommended to have an exposed copper pad in the location of the thermal heat gap filler, on the top layer of the carrier board.