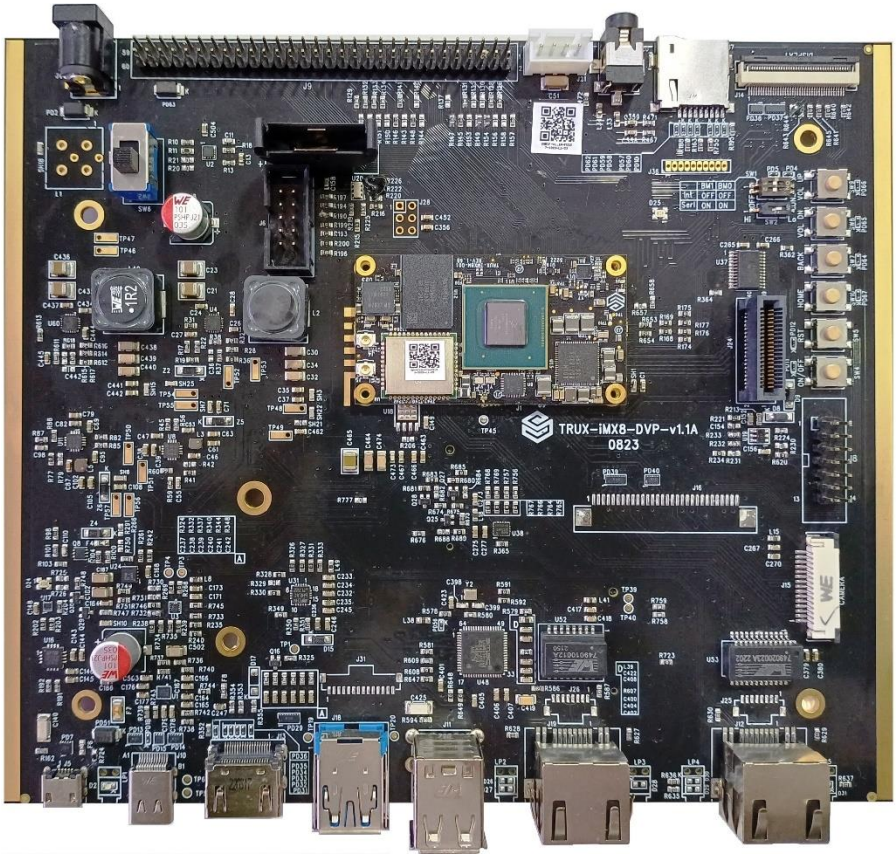
Datasheet for **TRUX-iMX8-DVP-v1.1**

(Development-board for SOM TRUX-iMX8M-Q01 & TRUX-iMX8MMini-Q01)



Rev 1-2

Status: Released

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Revision History

Revision	Date	Notes
1.0	January 3rd 2022	Initial Release
1.1	April 24th 2023	• 80 Pin connector replaced with 60 pin header. Removed GPIO connector (14 pin header) and RS232 connector (J22) and these signals shifted to 60 pin header (J9). • Power terminal block replaced with Power Jack. • NANO SIM connector replaced with Micro SIM connector. • CAN FD 4 pin terminal block replaced with relimate connector.
1.2	August 8th 2023	• Block diagram added for TRUX-iMX8-DVP-v1.1 (TRUX-iMX8MMini-Q01 assembled). • Booting switch represented. • Ordering Information added.

Acronyms and Abbreviations

Term	Meaning
I2S	Inter IC Sound
GPIO	General Purpose Input Output
B2B	Board to Board
LPDDR	Low Power Double Data Rate
eMMC	Embedded Multimedia Card
SD	Secure Digital
HDMI	High-Definition Multimedia Interface
USB	Universal Serial Bus
PCI	Peripheral Component Interconnect
MIPI	Mobile Industry Processor Interface
DSI	Display Serial Interface
CSI	Camera Serial Interface
I2C	Inter Integrated Circuit
ECSPI	Enhanced Configurable Serial Peripheral Interface
JTAG	Joint Test Action Group
UART	Universal Asynchronous Receiver Transmitter
CAN	Controller Area Network
PMIC	Power Management Integrated Circuit
SNR	Signal to Noise Ratio
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
SPDIF	Sony / Philips Digital Interface
SAI	Switch Abstraction Interface
CRC	Cyclic Redundancy Check
RGMII	Reduced Gigabit Media Independent Interface
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
ICMP	Internet Control Message Protocol
COL	Computer Oriented Language
PWM	Pulse Width Modulation
FIFO	First In First Out
OTG	On The Go
RDC	Resource Domain Controller
TZ	Trust Zone
OCRAM	On-chip RAM
HAB	High Assurance Boot
CAAM	Cryptographic acceleration and assurance
SNVS	Secure non-volatile storage
RTC	Real-time clock
SJC	Secure JTAG controller
ENET	Ethernet

1. Overview

1.1 General Information

TRUX-iMX8-DVP-v1.1 is a complete development board, utilizing all the TRUCRUX's TRUX-i.MX8M-Q01/ TRUX-i.MX8MMini-Q01 System-on-Module's features. It is assembled with a large variety of user and debug interfaces enabling it to serve as both a complete development kit or as a stand- alone end-product.

1.1.1 Supporting TRUCRUX products

- TRUX-iMX8M-Q01
- TRUX-iMX8MMini-Q01
- TRUX-iMX93-Q01 (Coming soon)

1.1.2 Supporting O.S

- Linux
- Android

1.1.3 Additional information

Board schematics and SW information is available on request.

For further information contact TRUCRUX support at info@trucrux.com

1.2 TRUX-iMX8-DVP-v1.1 Features

Board to Board Connector 90 pin (DF40C-90DS-0.4V(51)), compatible with the TRUX-i.MX8M-Q01/ TRUX-i.MX8MMini-Q01 [Mating connector on SOM: DF40C-90DP-0.4V(51)]

- Display
  - 1x MIPI DSI (4 lanes)
  - 1x HDMI 2.0a
- Touch panel interface
  - Capacitive - I2C interface
- Ethernet
  - 1x 1Gbps – RJ45
  - 1x 100Mbps – RJ45
- PCIe
  - 1x PCIe M2.0 KEY B – SSD
  - 1x PCIe M2.0 KEY M – 4G
- USB
  - 1x USB3.0/2.0 OTG Type C
  - 1x USB3.0 Host Type A
  - 2x USB2.0 Host Type A
- Audio
  - 3.5mm Headphones jack

- Micro SD-Card slot
- Camera
  - 2x MIPI CSI (4 lanes)
- CAN Bus
  - CAN FD 2.0
- Debug (UART)
  - Micro USB 2.0 - Type B
- RTC
  - RV-3028-C7 Chip
- Additional
  - UART, PWM, SAI, SPI, I2C, GPIOs - Header
  - General purpose LED, Buttons
- Power
  - 8V to 20V DC Input (Nom. 12V)
  - DC Power jack: 2.1mm ID x 5.5mm OD

1.3 Block Diagram of TRUX-iMX8-DVP-v1.1 (with TRUX-iMX8M-Q01)

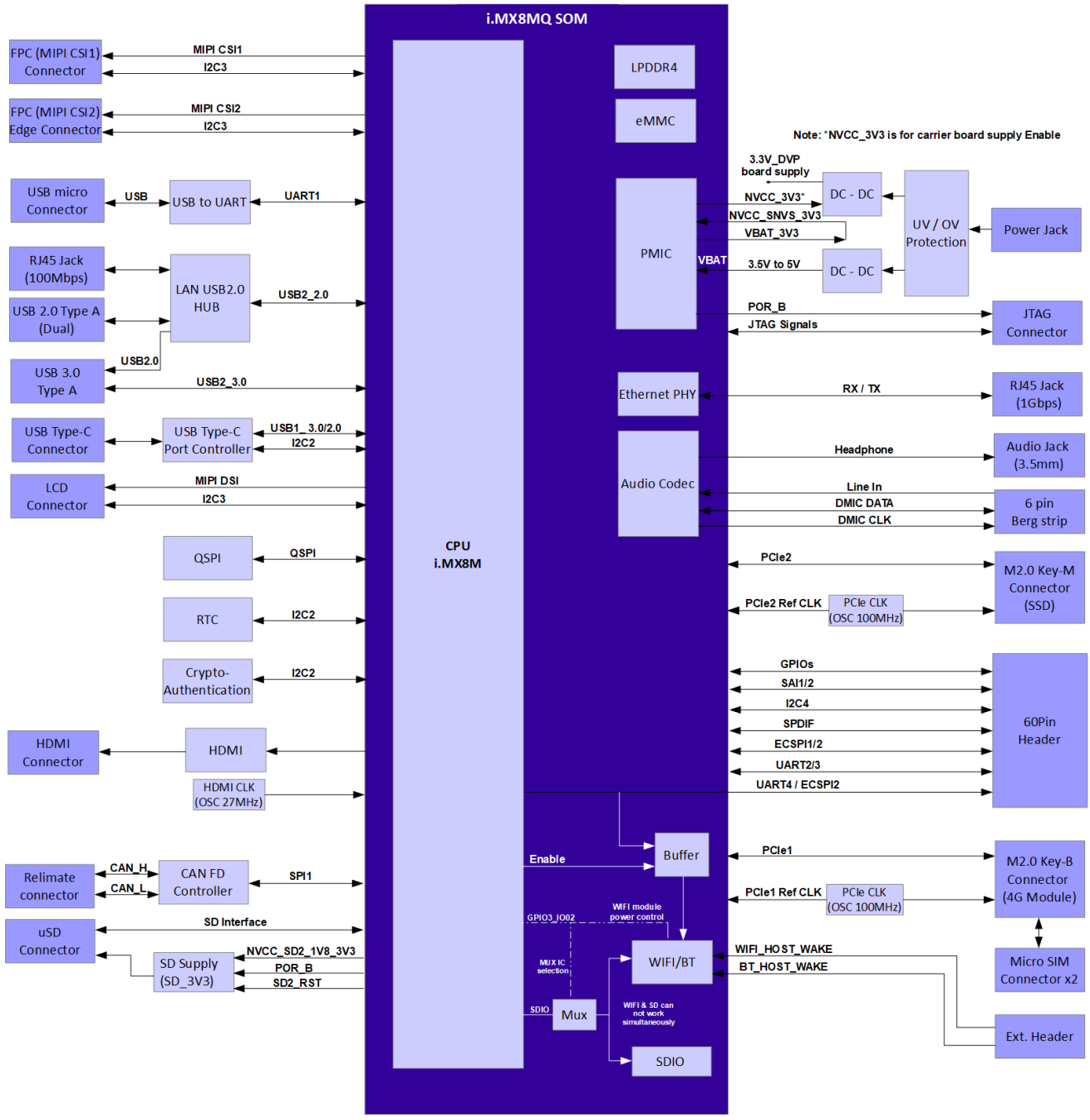

Figure1: Block Diagram of TRUX-iMX8-DVP-v1.1 (with TRUX-iMX8M-Q01)

1.4 Block Diagram of TRUX-iMX8-DVP-v1.1 (with TRUX-iMX8MMini-Q01)

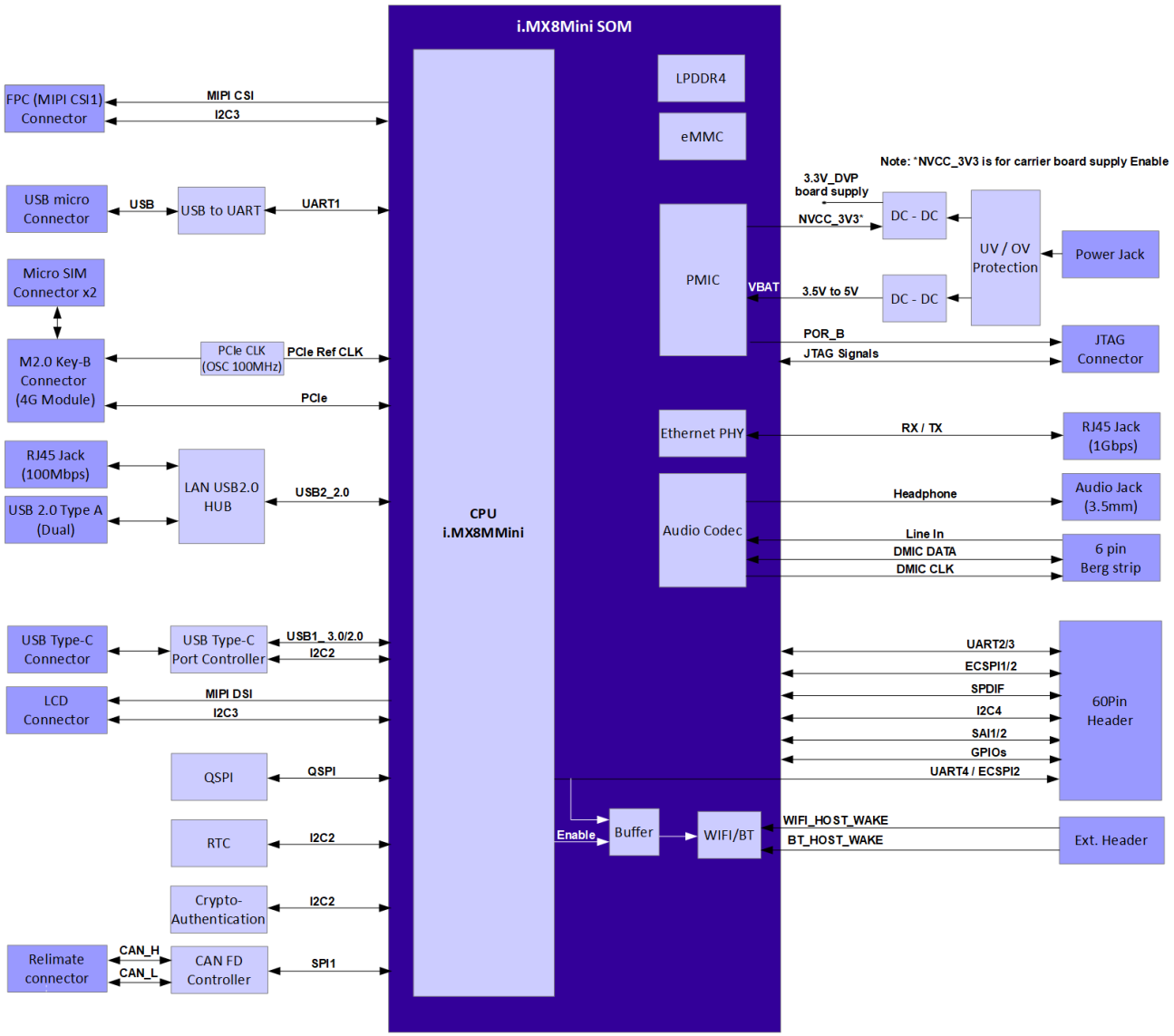

Figure2: Block Diagram of TRUX-iMX8-DVP-v1.1 (with TRUX-iMX8MMini-Q01)

1.5 SOM Comparison

B2B Pin Number	TRUX-iMX8MMini-Q01 Pin name	TRUX-iMX8MQ-Q01 Pin name	Remarks
J1.29	GPIO2_IO09_1V8	SD2_WP	Note: * Pin signals changed. These signals are different from TRUX-iMX8MQ-Q01
J1.35	CLKIN1_1V8	NAND_DATA07	
J1.37	CLKIN2_1V8	NAND_DATA06	
J1.41	GPIO1_IO07	NAND_RE_B	
J1.45	CLKOUT1_1V8	NAND_CLE	
J1.47	CLKOUT2_1V8	NAND_CE2_B	
J1.15	NVCC_SNVS_1V8 [1V8]	NVCC_SNVS [3V3]	Note: ** Voltage level changed. These signals are at different voltage from TRUX-iMX8MQ-Q01
J1.20	ONOFF_1V8 [1V8]	ONOFF [3V3]	
J1.22	PMIC_ON_REQ_1V8 [1V8]	PMIC_ON_REQ [3V3]	
J1.24	POR_B_1V8 [1V8]	POR_B [3V3]	
J1.26	PMIC_STBY_REQ_1V8 [1V8]	PMIC_STBY_REQ [3V3]	
J1.32	NAND_DATA01 [1V8]	NAND_DATA01 [3V3]	
J1.34	NAND_CE0_B [1V8]	NAND_CE0_B [3V3]	
J1.38	NAND_DQS [1V8]	NAND_DQS [3V3]	
J1.40	NAND_ALE [1V8]	NAND_ALE [3V3]	
J1.46	NAND_DATA03 [1V8]	NAND_DATA03 [3V3]	
J1.48	NAND_DATA00 [1V8]	NAND_DATA00 [3V3]	
J1.50	NAND_DATA02 [1V8]	NAND_DATA02 [3V3]	
J1.36	NC	NAND_READY_B	Note: *** Not Connected. These pins are not connected in TRUX-iMX8MMini-Q01
J1.39	NC	NAND_DATA04	
J1.42	NC	NAND_WP_B	
J1.43	NC	NAND_DATA05	
J1.44	NC	NAND_WE_B	
J1.54	NC	PCIE2_REF_CLKN	
J1.56	NC	PCIE2_REF_CLKP	
J1.63	NC	PCIE2_RXN	
J1.65	NC	PCIE2_RXP	
J1.66	NC	PCIE2_TXN	
J1.68	NC	PCIE2_TXP	
J1.72	NC	EN_VBAT_3V3	
J2	HDMI signals are not connected in TRUX-iMX8MMini-Q01 SoM		

J3	USB 3.0 TX/RX and MIPI CSI-2 signals are not connected in TRUX-iMX8MMini-Q01 SoM

1.6 Board Layout

TRUX-iMX8-DVP-v1.1 physical dimensions: 182 x 155.5 mm

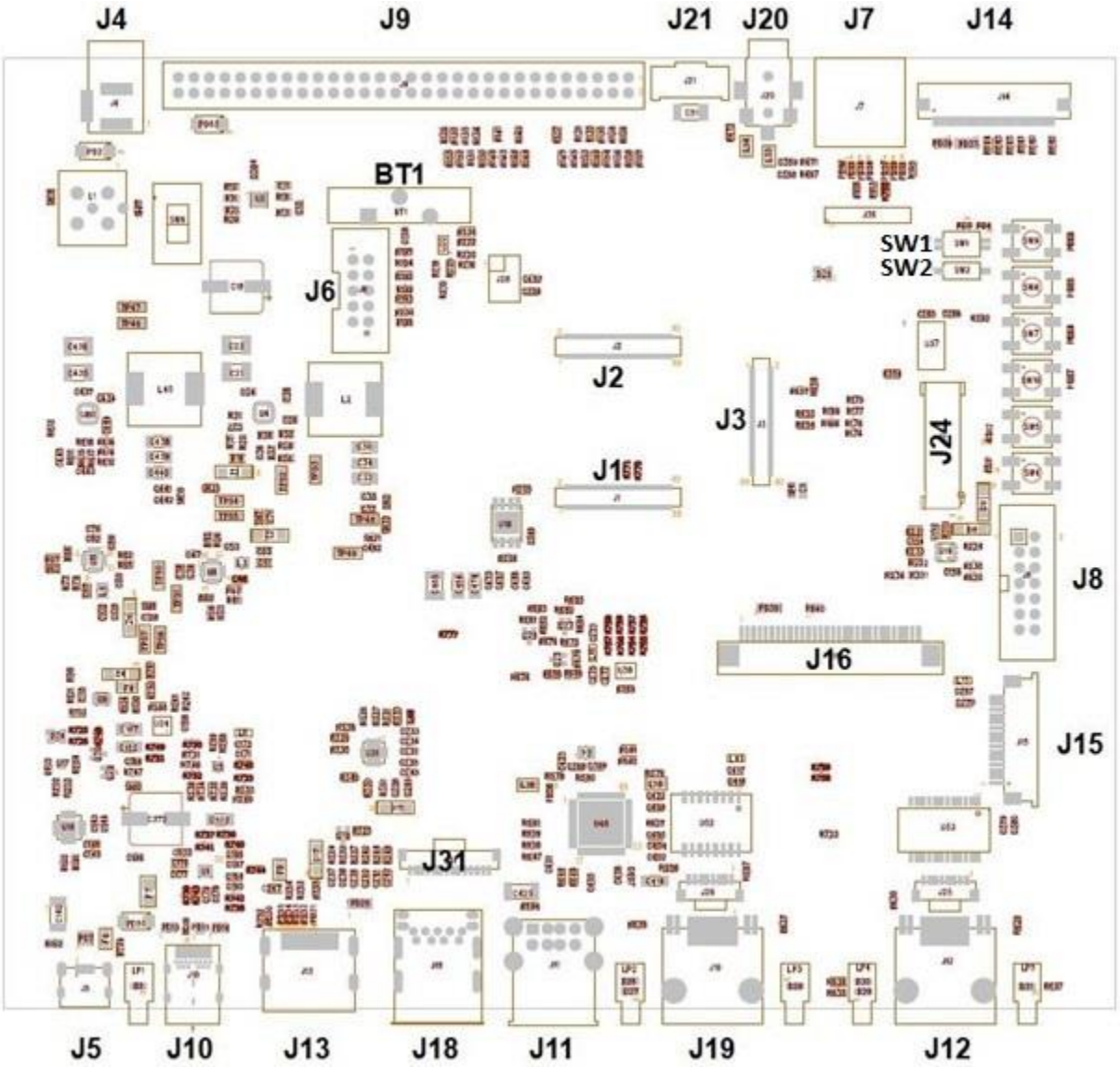

Figure3: Board layout – Top TRUX-iMX8-DVP-v1.1

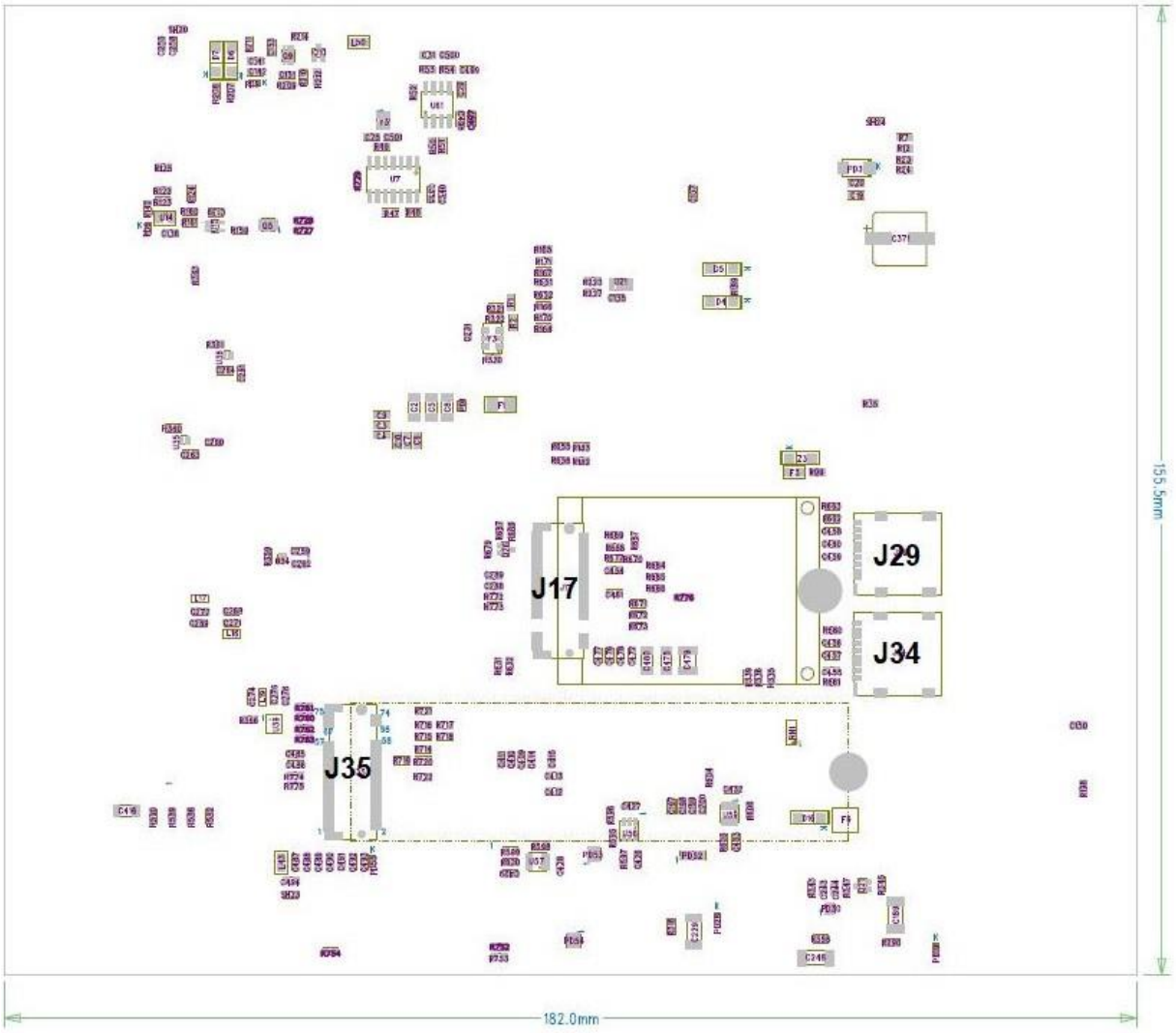

Figure4: Board layout – Bottom TRUX-iMX8-DVP-v1.1

1.7 TRUX-iMX8-DVP-v1.1 Connector Details

Below table lists all available connectors on the TRUX-iMX8-DVP-v1.1 Refer to chapter 2 for more detailed description and Pin-out of each connector.

Table 1-1 TRUX-iMX8-DVP-v1.1 connectors

Reference	Function	Description
BT1	Coin cell Holder	Coin Battery Holder 20mm
J1,J2,J3	SOM connector	B2B Plug 0.4mm, 90POS, SMT Gold
J4	Power in DC Jack	Input DC Power jack
J5	Micro USB connector	RCPT USB2.0 Micro B SMT
J6	JTAG connector	R/A Header 10POS, 2Row 2.54mm
J7	Micro SD Card connector	Micro SD SMD Push – Push 8POS SMT
J8	PMIC, WIFI, BT, GPIO connector	Header vertical 14 Pin, 2.54mm
J9	Edge connector: SPI, I2C, GPIO, SAI, UART, SPDIF signals	Header vertical 60 Pin, 2.54mm
J10	USB Type-C connector	RCP USB3.1 Type C, 24 Pin SMT
J11	USB 2.0 connector	RCPT USB2.0 Type A, Stack R/A
J12	RJ45 Jack	RJ45 Jack 1Gbps
J13	HDMI connector	RCPT HDMI 19POS SMT
J14	Display connector	FPC ZIF 40 Pin, 0.5mm Hinge
J15	Camera connector	FPC ZIF 15 Pin, 1mm Hinge
J16	Camera connector	FPC ZIF 30 Pin, 1mm Hinge
J17	M2.0 Connector PCIe 4G / 5G module	M2. 0 NGFF Key-B 67 Pin
J18	USB 3.0 connector	RCPT USB3.0 Type A, 9 Pin
J19	RJ45 Jack	RJ45 Jack 100Mbps
J20	Audio connector	Audio Jack 3.5mm
J21	CAN connector	Header vertical 2.5mm 4 pin
J24	Camera connector	High-speed edge card connector, vertical
J29,J34	SIM connector	Micro SIM card connector
J31	SATA USB connector	Relimate SMD 14 Pin, 1mm
J35	M2.0 Connector PCIe SSD	M2. 0 NGFF Key-M 67 Pin

2. Detailed Description

2.1 Overview

This chapter details the TRUX-iMX8-DVP-v1.1 features and external interfaces, some of which are driven directly by the TRUX-i.MX8M-Q01/ TRUX-i.MX8MMini-Q01. Please refer to the SOM data sheet for more information. Table 2-1 describes this chapter table header and acronyms used.

Table 2-1: Acronyms used on tables column header

Column	Pin name	Meaning
Pin#	X	Pin number on a connector
Type		Pin type & direction
	I	Input
	O	Output
	DS	Differential Signal
	A	Analog
	P	Power
Signal		TRUX-iMX8-DVP-v1.1 schematic signal name
Description		Pin functionality description

2.2 TRUX-iMX8-DVP-v1.1 Interfaces

2.2.1 SOM

TRUX-iMX8-DVP-v1.1 features Board to Board Connector 90 pin mating connector to connect with the TRUX-i.MX8M-Q01/ TRUX-i.MX8MMini-Q01 System-on-module. Please refer to the SOM module datasheet for a complete signal description and pin-out of SOM Connectors.

2.3 Standard External Interfaces

2.3.1 USB Type C OTG (J10)

TRUX-iMX8-DVP-v1.1 features a GPIO controlled switch which routes SOM USB Type C OTG connector. When using TRUX-i.MX8M-Q01/ TRUX-i.MX8MMini-Q01 SOMs, pins are routed to USB Type C OTG connector providing one USB3.0/2.0 OTG port.

Table 2-2: USB Type-C OTG connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
A2	SSTX1P	DSO	SuperSpeed diff. pair #1, TX, positive
A3	SSTX1N	DSO	SuperSpeed diff. pair #1, TX, negative
A5	CC1	IO	Configuration channel
A6	USB1_DP	DSIO	Non-SuperSpeed diff. pair, pos. 1, positive
A7	USB1_DN	DSIO	Non-SuperSpeed diff. pair, pos. 1, negative
A8	TP5	IO	Sideband use (SBU)
A10	SSRXN2	DSI	SuperSpeed diff. pair #4, RX, negative

A11	SSRXP2	DSI	SuperSpeed diff. pair #4, RX, positive
B2	SSTXP2	DSO	SuperSpeed diff. pair #3, TX, positive
B3	SSTXN2	DSO	SuperSpeed diff. pair #3, TX, negative
B5	CC2	IO	Configuration channel
B6	USB1_DP	DSIO	Non-SuperSpeed diff. pair, pos. 2, positive
B7	USB1_DN	DSIO	Non-SuperSpeed diff. pair, pos. 2, negative
B8	TP6	IO	Sideband use (SBU)
B10	SSRXN1	DSI	SuperSpeed diff. pair #2, RX, negative
B11	SSRXP1	DSI	SuperSpeed diff. pair #2, RX, positive
A4, B4, A9, B9	USB_SNC	P	Bus power
A1, B1, B12, A12	GND	P	Ground

Note: With SOM TRUX-iMX8MMini-Q01, only USB2.0 is applicable.

2.3.2 USB Host Type A (J18 & J11)

TRUX-iMX8-DVP-v1.1 has an additional two USB 2.0 Host port and one USB 3.0 Host port is exported through USB Type A connector.

Table 2-3: USB 3.0 Type-A connector Pin-out (J18)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	USB_DM	DSIO	USB 2.0 Data -
3	USB_DP	DSIO	USB 2.0 Data +
5	USB_RXN	DSI	SuperSpeed receiver
6	USB_RXP	DSI	SuperSpeed receiver
8	USB_TXN	DSO	SuperSpeed transmitter
9	USB_TXP	DSO	SuperSpeed transmitter
1	USB_VBUS4	P	+5V power
4, 7	GND	P	Ground
10	NC	-	Not connected

Note: USB3.0 is applicable only for SOM TRUX-iMX8M-Q01, not for TRUX-iMX8MMini-Q01

Table 2-4: USB 2.0 Type-A connector Pin-out (J11)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	USB_DM1	DSIO	USB 2.0 Data -
3	USB_DP1	DSIO	USB 2.0 Data +
6	USB_DM2	DSIO	USB 2.0 Data -
7	USB_DP2	DSIO	USB 2.0 Data +
1	USB_VBUS1	P	+5 V power
5	USB_VBUS2	P	+5 V power
4, 8	GND	P	Ground

2.3.3 Micro USB2.0 Type B (UART Debug J5)

Table 2-5: USB2.0 Micro Type B Device connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	USB3_DN	DSIO	USB 2.0 Data -
3	USB3_DP	DSIO	USB 2.0 Data +
1	VCC	P	+5 V power
4	GND	P	Ground

2.3.4 SATA Connector (J31)

Table 2-6: SATA 2.0 connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	USB_TXP	DSIO	SATA Transmit Lane diff. Positive
3	USB_TXN	DSIO	SATA Transmit Lane diff. Negative
5	USB_RXP	DSIO	SATA Receive Lane diff. Positive
6	USB_RXN	DSIO	SATA Receive Lane diff. Negative
8	USB_DM	DSIO	Data -
9	USB_DP	DSIO	Data +
11, 12	VDD_3V3	P	Power
13, 14	VDD_5V	P	Power
1, 4, 7, 10	GND	P	Ground

2.3.5 HDMI Connector (J13)

HDMI CLK and Data lines (TMDS type) should be terminated using 604-Ohm resistors. Termination should be applied after HDMI analog core is powered. Power supply VDD_PHY_1V8 from Board-to-board Connector J2 can be used for the termination control. See below Figure for illustration of the termination scheme.

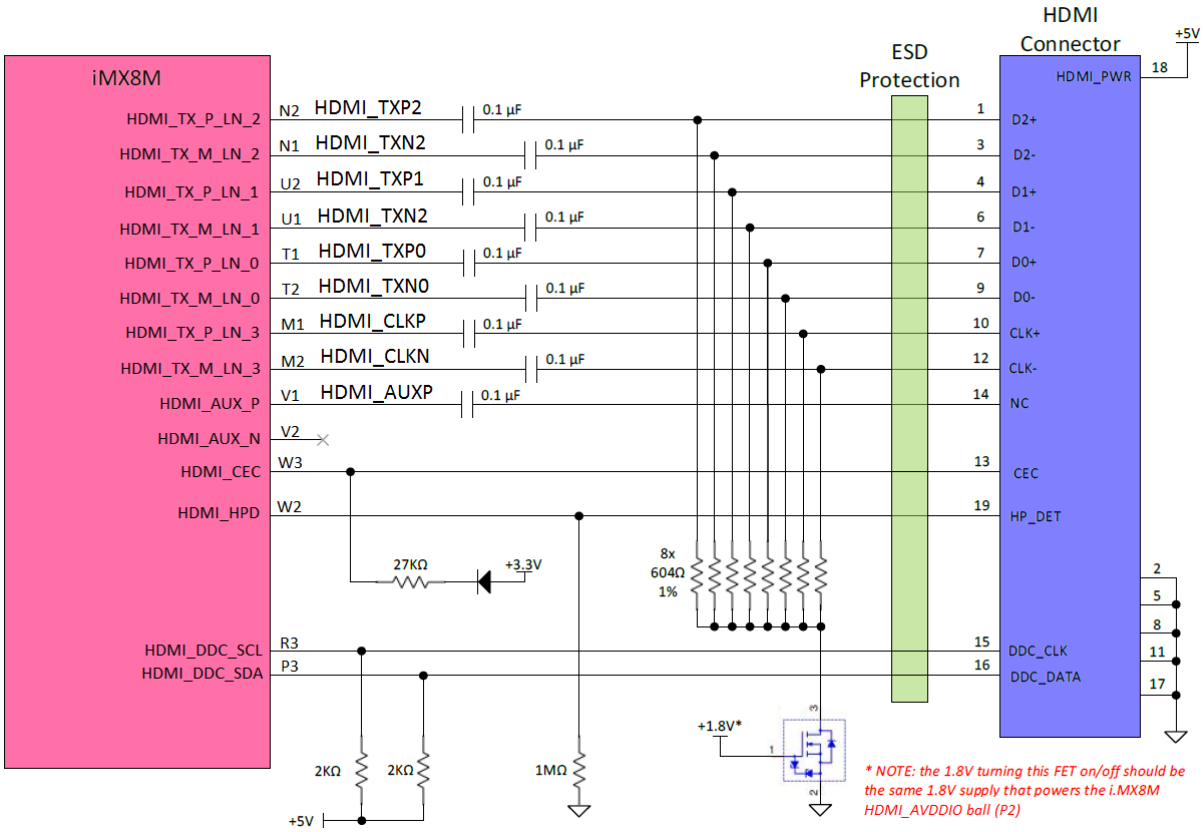

Figure5: HDMI Interfacing *(Reference NXP)*

Table 2-7: HDMI connector Pin-out (J13)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	HDMI_TXP2_CN	DSO	HDMI TMDS diff. pair #2, TX, positive
3	HDMI_TXN2_CN	DSO	HDMI TMDS diff. pair #2, TX, negative
4	HDMI_TXP1_CN	DSO	HDMI TMDS diff. pair #1, TX, positive
6	HDMI_TXN1_CN	DSO	HDMI TMDS diff. pair #1, TX, negative
7	HDMI_TXP0_CN	DSO	HDMI TMDS diff. pair #0, TX, positive
9	HDMI_TXN0_CN	DSO	HDMI TMDS diff. pair #0, TX, negative
10	HDMI_CLKP_CN	DSO	HDMI TMDS diff. Clock; positive
12	HDMI_CLKN_CN	DSO	HDMI TMDS diff. Clock; negative
13	HDMI_CEC_CN	IO	Consumer Electronics Control
14	HDMI_UTILITY/HEAC+_CN	I	HDMI_Utility; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Positive
15	HDMI_DDC_SCL_CN	O	I2C Serial Clock for DDC
16	HDMI_DDC_SDA_CN	IO	I2C Serial Data for DDC
19	HDMI_HPD/HEAC-_CN	I	HDMI Hot Plug Detect; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Negative

18	DCDC_5V_CN	P	Power
2,5,8,11,17	GND	P	Ground

Note: HDMI is applicable only for SOM TRUX-iMX8M-Q01, not for TRUX-iMX8MMini-Q01

2.3.6 Ethernet (J19 & J12)

Table 2-8: Internal PHY 10/100BaseT RJ45 connector Pin-out (J19)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	TRX0_P_100	DSIO	Bi-directional diff. pair 1 positive
2	TRX0_N_100	DSIO	Bi-directional diff. pair 1 negative
3	TRX1_P_100	DSIO	Bi-directional diff. pair 2 positive
6	TRX1_N_100	DSIO	Bi-directional diff. pair 2 negative
12	LINK	O	Activity LED
10	SPEED	O	Activity LED
9,11	VDD_3V3	P	Power
4,5,7,8	NC	-	Not connected

Table 2-9: External PHY 10/100/1000BaseT RJ45 connector Pin-out (J12)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	TRX0_P	DSIO	Bi-directional diff. pair 1 positive
2	TRX0_N	DSIO	Bi-directional diff. pair 1 negative
3	TRX1_P	DSIO	Bi-directional diff. pair 2 positive
6	TRX1_N	DSIO	Bi-directional diff. pair 2 negative
4	TRX2_P	DSIO	Bi-directional diff. pair 3 positive
5	TRX2_N	DSIO	Bi-directional diff. pair 3 negative
7	TRX3_P	DSIO	Bi-directional diff. pair 4 positive
8	TRX3_N	DSIO	Bi-directional diff. pair 4 negative
9	LED_LINK10_100	O	Activity LED
10	LED_LINK1000	O	Activity LED
11	LED_ACT	O	Activity LED
12	GND	P	Ground

2.3.7 Micro SD Card (J7)

Table 2-10: uSD card slot connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	SDIOMUX_SD2_DATA2	IO	SD Parallel Data2
2	SDIOMUX_SD2_DATA3	IO	SD Parallel Data3
3	SDIOMUX_SD2_CMD	IO	SD Command
5	SDIOMUX_SD2_CLK	I	SD Clock
7	SDIOMUX_SD2_DATA0	IO	SD Parallel Data0
8	SDIOMUX_SD2_DATA1	IO	SD Parallel Data1

9	SD2_Ncd	O	SD Card Detect
4	SD_3V3	P	SD card 3.3V supply
6	GND	P	Digital Ground
10,11,12,13	NC	-	Not Connected

2.3.8 3.5mm Audio Jack Connector Pin-out (J20)

Table 2-11: Headphone out Jack connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	HPROUT	AO	Headphone out Right
3	HPLOUT	AO	Headphone out Left
4	HPOUTFB	AP	Analog ground return for audio
1	NC	-	Not Connected

2.3.9 CAN BUS Interface (J21)

Table 2-12: CAN BUS Relimate connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	CAN-H	IO	CAN Bus High
3	CAN-L	IO	CAN Bus Low
4	GND	P	Ground
1	NC		Not connected

2.4 Board External Interfaces

TRUX-iMX8-DVP-v1.1 exposes two, independent PCI Express GEN 2 single lane interfaces. Each PCI Express port requires an external 100MHz PCIe compliant reference clock.

- Dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application.
- Port solution includes the controller, an analog PHY macro, and application logic to source and sink data.
- PCI Express base specification 2.1 with maximum 5.0Gbps lane rate.
- Native PCIe PM Mechanisms.

2.4.1 PCIe with M2.0 Key – B (J17)

Table 2-13: PCIe M2.0 Key – B connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	CONFIG_3	IO	Host Configuration
6	FULL_CARD_POWER_OFF#	IO	Card Power OFF
7	USB_DP	DSIO	USB 2.0 Data +
8	W_DISABLE1#	IO	Activity Signal1

9	USB_DM	DSIO	USB 2.0 Data -
10	WWAN_LED#	IO	Activity Signal
21	CONFIG_0	IO	Host Configuration
23	WAKE_ON_WAN#	IO	PCIe WAKE
25	DPR	IO	Activity Signal
26	W_DISABLE2#	IO	Activity Signal2
30	USIM1_RST	IO	SIM1 Reset
32	USIM1_CLK	O	SIM1 Clock
34	USIM1_DATA	IO	SIM1 Data
36	USIM1_VDD	P	SIM1 Supply
40	USIM2_DET	I	SIM2 Detect
41	PCIE_RX_M	DSI	PCIe Receive Lane diff. Negative
42	USIM2_DATA	IO	SIM2 Data
43	PCIE_RX_P	DSI	PCIe Receive Lane diff. Positive
44	USIM2_CLK	O	SIM2 Clock
46	USIM2_RST	O	SIM2 Reset
47	PCIE_TX_M	DSO	PCIe Transmit Lane diff. Negative
48	USIM2_VDD	P	SIM2 Supply
49	PCIE_TX_P	DSO	PCIe Transmit Lane diff. Positive
50	PCIE_RST_N	O	PCIe Reset
52	PCIE_CLKREQ_N	DSO	PCIe Clock Request
53	PCIE_REFCLK_M	DSO	PCIe Clock diff. Negative; 100MHz HCSL
54	PCIE_WAKE_N	IO	PCIe WAKE
55	PCIE_REFCLK_P	DSO	PCIe Clock diff. Positive; 100MHz HCSL
60	WLAN_PA_EN	O	PCIe WAKE
66	USIM1_DET	I	SIM1 Detect
67	RESET#	O	Device Reset
68	ANT_CONFIG	IO	Antenna Configuration
69	CONFIG_1	IO	Host Configuration
75	CONFIG_2	IO	Host Configuration
2,4,70,72,74	Power	P	Power
3,5,11,27,33, 39,45, 51,57,71,73,7 6	GND	P	Ground
20,22,24,28,2 9,31,35,37, 38,56,58,59,6 1,62,63,64,65	NC	-	Not connected

2.4.2 PCIe with M2.0 Key – M (J35)

Table 2-14: PCIe M2.0 Key – M connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
1	CONFIG_3	IO	Host Configuration
10	DAS/DSS	IO	Activity Signal
21	CONFIG_0	IO	Host Configuration
38	DEV_SLP	IO	Device Sleep
41	PCIE_RX0_M	DSI	PCIe Receive Lane diff. Negative
43	PCIE_RX0_P	DSI	PCIe Receive Lane diff. Positive
47	PCIE_TX0_M	DSI	PCIe Transmit Lane diff. Negative
49	PCIE_TX0_P	DSI	PCIe Transmit Lane diff. Positive
50	PCIE_RST_N	DSI	PCIe Reset
52	PCIE_CLKREQ_N	O	PCIe Clock Request
53	PCIE_REFCLK_M	DSO	PCIe Clock diff. Negative; 100MHz HCSL
54	PCIE_WAKE_N	IO	PCIe WAKE
55	PCIE_REFCLK_P	DSO	PCIe Clock diff. Positive; 100MHz HCSL
68	SUSCLK	O	32.768 kHz clock
69	CONFIG_1	IO	Host Configuration
75	CONFIG_2	IO	Host Configuration
2,4,12,14,16, 18,70,72,74	Power	P	Power
3,9,15,27,33, 39,45, 51,57,71,73,7 6	GND	P	Ground
5,6,7,8,11,13, 17,19,20, 22,23,24,25,2 6,28,29,30, 31,32,34,35,3 6,37,40 ,42,44,46,48, 56,58,67	NC	-	Not connected

2.4.3 MIPI DSI (J14)

Table 2-15: MIPI DSI connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	DSI_DN0	DSIO	Display Port Lane0 diff. negative
3	DSI_DP0	DSIO	Display Port Lane0 diff. positive
5	DSI_DN1	DSIO	Display Port Lane1 diff. negative

6	DSI_DP1	DSIO	Display Port Lane1 diff. positive
8	DSI_CLKN	DSIO	Display CLK Negative
9	DSI_CLKP	DSIO	Display CLK Positive
11	DSI_DN2	DSIO	Display Port Lane2 diff. negative
12	DSI_DP2	DSIO	Display Port Lane2 diff. positive
14	DSI_DN3	DSIO	Display Port Lane3 diff. negative
15	DSI_DP3	DSIO	Display Port Lane3 diff. positive
24	DIS_TE	I	Display Tearing Effect
25	DIS_RST	I	Display Reset
26	DIS_BUFF_EN	I	GPIO
30	TOUCH_RST	I	Touch Reset
31	TOUCH_IRQ	I	Touch IRQ
33	MIPI_DSI_SCL	I	I2C SCL
34	MIPI_DSI_SDA	IO	I2C SDA
40	DIS_PWM	O	PWM
18,19,21,32,35,36,37,38,39	VDD_3V3	P	Power
1,4,7,10,13,16,17,20,22,23,27,28,29	GND	P	Ground
24, 26	NC		Not Connected

2.4.4 MIPI CSI (J15 & J16)

Table 2-16: MIPI CSI connector (15 Pin) Pin-out (J15)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	CSI_P1_DN0	DSIO	Camera1 Port Lane0 diff. negative
3	CSI_P1_DP0	DSIO	Camera1 Port Lane0 diff. positive
5	CSI_P1_DN1	DSIO	Camera1 Port Lane1 diff. negative
6	CSI_P1_DP1	DSIO	Camera1 Port Lane1 diff. positive
8	CSI_P1_CKN	DSO	Camera1 CLK Negative
9	CSI_P1_CKP	DSO	Camera1 CLK Positive
11	CAM1_PWREN	O	Camera1 Enable
12	CAM1_SYNC	O	Camera1 Clock
13	CAM1_I2C_SCL	IO	I2C SCL
14	CAM1_I2C_SDA	O	I2C SDA
15	VDD_3V3	P	Power
1,4,7,10,16,17	GND	P	Ground

Table 2-17: MIPI CSI connector (30 Pin) Pin-out (J16)

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description

2	CSI_P1_DN0	DSIO	Camera1 Port Lane0 diff. negative
3	CSI_P1_DP0	DSIO	Camera1 Port Lane0 diff. positive
5	CSI_P1_DN1	DSIO	Camera1 Port Lane1 diff. negative
6	CSI_P1_DP1	DSIO	Camera1 Port Lane1 diff. positive
8	CSI_P1_CKN	DSIO	Camera1 CLK negative
9	CSI_P1_CKP	DSIO	Camera1 CLK Positive
11	CSI_P1_DN2	DSIO	Camera1 Port Lane2 diff. negative
12	CSI_P1_DP2	DSIO	Camera1 Port Lane2 diff. positive
14	CSI_P1_DN3	DSIO	Camera1 Port Lane3 diff. negative
15	CSI_P1_DP3	DSIO	Camera1 Port Lane3 diff. positive
17	CAM1_I2C_SDA	O	I2C SDA
18	CAM1_I2C_SCL	IO	I2C SCL
20	CAM1_SYNC	O	Camera1 Clock
22	CAM1_PWREN	O	Camera1 Enable
23	CAM1_RST	I	Camera1 Reset
24	CAM1_OPT	I	Activity Signal
25	CAM1_TRIG	I	Activity Signal
27,28	VDD_3.3V	P	Power
29,30	VDD_1.8V	P	Power
1,4,7,10,13,16,19,21,31,32	GND	P	Ground
26	NC	-	Not connected

2.4.5 60 Pin Edge Connector (J9)

Table 2-18: General Purpose IO connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
3	GPIO1_IO03	IO	GPIO
4	GPIO1_IO05	IO	GPIO
5	GPIO1_IO11	IO	GPIO
6	SAI1_RXD1	IO	GPIO
7	SAI1_RXD0	IO	GPIO
8	SAI1_RXD2	IO	GPIO
9	SAI1_RXD4	IO	GPIO
10	SAI1_TXD1	IO	GPIO
11	SAI1_RXD5	IO	GPIO
12	SAI1_TXD5	IO	GPIO
13	SAI1_TXD3	IO	GPIO
14	UART2_RXD	IO	GPIO
15	UART3_RXD	IO	GPIO

16	UART3_TXD	IO	GPIO
17	ECSPI1_MOSI	IO	GPIO
18	ECSPI1_MISO	O	GPIO
19	ECSPI1_SS0	IO	GPIO
20	ECSPI1_SCLK	IO	GPIO
21	UART2_TXD	IO	GPIO
22	SAI1_TXD6	IO	GPIO
23	SAI1_TXD2	IO	GPIO
24	SAI1_TXD7	IO	GPIO
25	SAI1_TXD4	IO	GPIO
26	SAI1_TXD0	IO	GPIO
27	SAI1_RXD7	IO	GPIO
28	SAI1_RXD6	IO	GPIO
29	SAI1_RXD3	IO	GPIO
30	SAI2_TXD	IO	GPIO
31	SAI2_RXD	IO	GPIO
32	SAI2_TXC	IO	GPIO
33	SAI2_MCLK	IO	GPIO
34	SAI2_TXFS	IO	GPIO
35	SAI2_RXC	IO	GPIO
36	SAI2_RXFS	IO	GPIO
37	ECSPI2_SS0	IO	GPIO
38	ECSPI2_SCLK	IO	GPIO
39	ECSPI2_MISO	IO	GPIO
40	ECSPI2_MOSI	IO	GPIO
41	SPDIF_TX	IO	GPIO
42	SPDIF_EXT_CLK	IO	GPIO
43	I2C_OUT_SDA	IO	Camera I2C SDA
44	I2C_OUT_SCL	O	Camera I2C SCL
46	NVCC_3V3	P	Power
49,50,51,52,53, 54	VSYS_MUX	P	Power
1,2,45,57,58,59, 60	GND	P	Ground
47,48,55,56	NC	-	Not connected

2.4.6 JTAG Connector (J6)

Table 2-19: JTAG connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
2	JTAG_TMS	O	Test Mode Select

4	JTAG_TCK	O	Test Clock
6	JTAG_TDO	O	Test Data Output
8	JTAG_TDI	I	Test Data Input
9	TRSET	O	Test Reset
10	RESET	O	Device Reset
1	VCC	P	Power
3,5,7,9	GND	P	Ground

2.4.7 SOM Control Connector (J8)

Table 2-20: SOM control connector Pin-out

Pin #	TRUX-iMX8-DVP-v1.1 Signal	Type	Description
4	GPIO1_IO02	IO	GPIO
5	ONOFF	I	SoC ON-OFF
6	GPIO1_IO00	IO	GPIO
7	PMIC_ON_REQ	I	SOM Power On Request; Active Low; Driven by SOM PMIC
8	WIFI_HOST_WAKE	I	SOM WIFI module WIFI host wake
9	POR_B	I	SOM Power On Reset; Active Low; Driven by SOM PMIC
10	BT_HOST_WAKE	I	SOM WIFI module Bluetooth host wake
11	PMIC_STBY_REQ	I	SOM PMIC Standby Request; Active Low; Driven by SOM PMIC
12	GPIO1_IO08	IO	GPIO
1,3	NVCC_3V3	P	Power
2	NVCC_SNVS_3V3	P	Power
13	EN_VBAT_3V3	P	Power
14	GND	P	Ground

2.4.8 Control Buttons

2.4.8.1 Boot Select (SW1)

The Boot select switch SW1 sets the SOM boot source & sequence. Refer to the SOM datasheet for detailed boot description.

Table 2-21: Boot Select modes (SW1)

SW Config.	BM1	BM0	Description
1-4: OFF; 2-3: OFF	0	1	Internal Boot
1-4: ON; 2-3: ON	1	0	Serial Downloader
1-4: ON; 2-3: OFF	0	0	Boot From Fuse
1-4: OFF; 2-3: ON	1	0	Reserve

2.4.8.2 Boot Flash Select (SW2) & Ext. switch

The Boot select switch SW2 and Ext. Switch sets the SOM flash source & sequence. Refer to the SOM data sheet for detailed Boot description.

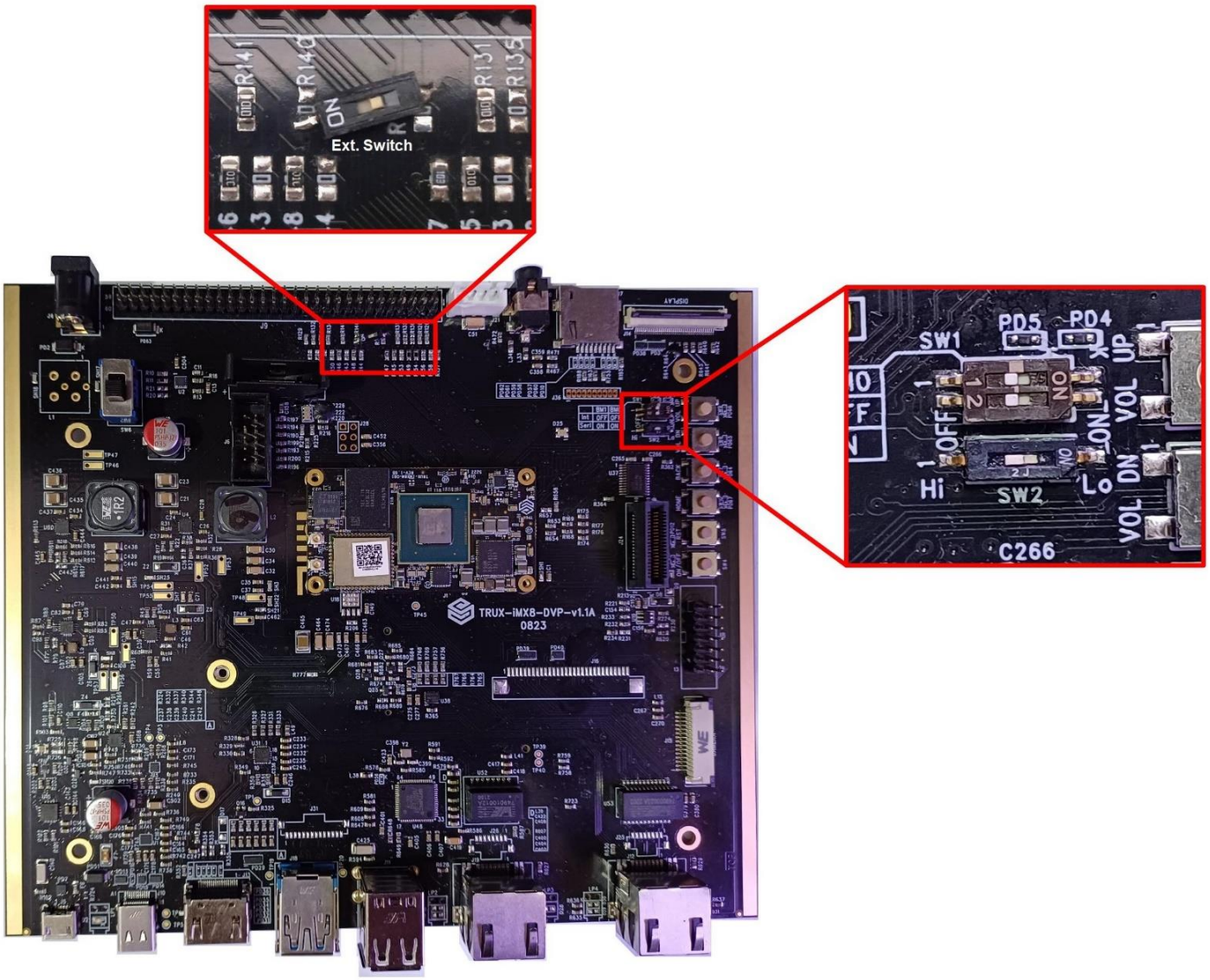

Figure6: Booting Switches representation

The TRUX SOM will boot on DVP as per below switch settings:-

Table 2-22: Boot Select modes (SW2 & Ext. SW)

TRUX-iMX8M-Q01		
Switches	**Position**	**Boot from**
SW2	ON	**eMMC**
EXT SW	Don't Care	
SW2	OFF	**SD**
EXT SW	Don't Care	

TRUX-iMX8MMini-Q01		
Switches	**Position**	**Boot from**
SW2	ON	**eMMC**
EXT SW	OFF	
SW2	OFF	**SD**
EXT SW	ON	

2.4.8.3 ONOFF Button (SW4)

The ON/OFF Button supports following modes:

1. In OFF mode: A brief button press causes the internal power management state machine to change state to ON.
2. In ON mode: A brief button press generates an interrupt (intended to initiate a software-controllable power-down). An approximate 5 second or more button press causes a forced OFF.

2.4.8.4 Reset Button (SW5)

A press on SW5 will perform a system reset of the SOM.

2.4.8.5 LED Indications (D2)

D2 indicates that TRUX-iMX8-DVP-v1.1 Carrier VSYS power is ON

2.4.9 Power (J4)

The TRUX-iMX8-DVP-v1.1 is powered by a +12V power supply, connected through a 2.1mm power jack.

2.4.9.1 RTC Backup Battery (BT1)

The TRUX-iMX8-DVP-v1.1 features BT1, a battery holder with a Coin cell 20mm (3V) as a backup power on board RV-3028-C7 RTC Module.

3. Electrical Environmental Specifications

3.1 Absolute Maximum Electrical Specifications

Table 3-1: DC Power Input absolute maximum electrical specifications

Supply	Min	Nom	Max
Main Power Supply, DC-IN	-0.3VDC	12VDC	20VDC

3.2 Operational Electrical Specifications

Table 3-2: DC Power Input Operational electrical specifications

Supply	Min	Nom	Max
Main Power Supply, DC-IN	8VDC	12VDC	18VDC

3.3 Environmental specifications

Table 3-3: Environmental specifications

Parameter	Min	Max
Commercial operating temperature range	0^0C	+70^0C
MTBF	>10kHRS	
Relative humidity, Operational	10%	90%
Relative humidity, Storage	5%	95%

4. Ordering Information

	Easy Kit	Explorer Kit
Part number	TRUX-ESK-8M -Q01 TRUX-ESK-8MMini-Q01 TRUX-ESK-93-Q01	TRUX-EPK-8M-Q01 TRUX-EPK-8MMini-Q01 TRUX-EPK-93-Q01
Included SOM	TRUX-iMX8MQ-Q01 / TRUX-iMX8MMini-Q01	TRUX-iMX8MQ-Q01 / TRUX-iMX8MMini-Q01
Included Development board	TRUX-iMX8-DVP	TRUX-iMX8-DVP
Display	x	10” TFT
Touch panel	x	Capacitive
Micro-USB debug cable	x	√
Ethernet cable	x	√
12V power supply	√	√
Boot / Rescue SD Cards	x	√
Heatsink	√	√
Camera module	x	Optional